

Zahari, Finn; Park, Seongae; Mahadevaiah, Mamathamba K.; Wenger, Christian; Kohlstedt, Hermann; Ziegler, Martin

Redox-based bi-layer metal oxide memristive devices

Original published in: Bio-inspired information pathways : from neuroscience to neurotronics. - Cham : Springer International Publishing, (2024), p. 87 - 114.

Original published: [2024]

ISSN: 2520-8543; 2520-8535

ISBN: 978-3-031-36705-2; 978-3-031-36704-5

DOI: [10.1007/978-3-031-36705-2_3](https://doi.org/10.1007/978-3-031-36705-2_3)

[Visited: 2026-02-03]



This work is licensed under a [Creative Commons Attribution 4.0 International license](https://creativecommons.org/licenses/by/4.0/). To view a copy of this license, visit <https://creativecommons.org/licenses/by/4.0/>

Redox-Based Bi-Layer Metal Oxide Memristive Devices



Finn Zahari, Seongae Park, Mamathamba K. Mahadevaiah,
Christian Wenger, Hermann Kohlstedt, and Martin Ziegler

Abstract In a memristor or a so-called memristive device, the resistance state depends on the previous charge flow through the device. The new resistance state is stored and classifies a memristor as a non-volatile memory device. This likewise unique and simple feature qualifies memristive devices as attractive compartments with regard to the development of a universal memory and beyond von Neumann computing architectures, including in-memory computing and neuromorphic circuits. In this chapter, we present studies on two kinds of bi-layer metal oxide memristive devices with the layer sequences Nb/NbO₂/Al₂O₃/Nb_xO_y/Au and TiN/TiO_x/HfO_x/Au, either prepared by reactive DC-magnetron sputtering, etching and optical lithography. It is shown that the memristive properties of such devices can be engineered, which enables tailoring of the memristive devices for particular applications.

F. Zahari (✉) · H. Kohlstedt
Nanoelectronics, Faculty of Engineering, Kiel University, 24143 Kiel, Germany
e-mail: fnz@tf.uni-kiel.de

H. Kohlstedt
e-mail: hko@tf.uni-kiel.de

S. Park · M. Ziegler
Department of Electrical Engineering and Information Technology, Technische Universität
Ilmenau, 98693 Ilmenau, Germany
e-mail: seongae.park@tu-ilmenau.de

M. Ziegler
e-mail: martin.ziegler@tu-ilmenau.de

Institute of Micro and Nanotechnologies MacroNano, Technische Universität Ilmenau, 98693
Ilmenau, Germany

M. K. Mahadevaiah
IHP Leibniz-Institut für innovative Mikroelektronik, Frankfurt, Germany
e-mail: kalishettyhalli@ihp-microelectronics.com

C. Wenger
IHP Leibniz-Institut für innovative Mikroelektronik, Frankfurt/Oder, Germany
e-mail: wenger@ihp-microelectronics.com

© The Author(s) 2024

M. Ziegler et al. (eds.), *Bio-Inspired Information Pathways*, Springer Series
on Bio- and Neurosystems 16, https://doi.org/10.1007/978-3-031-36705-2_3

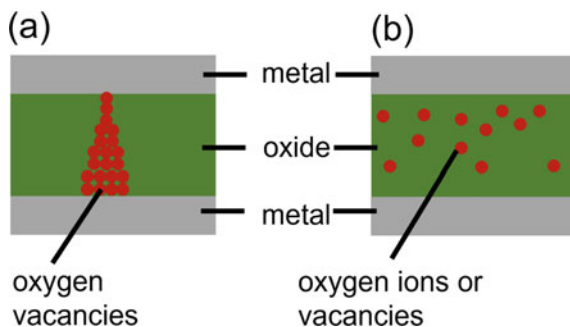
1 Introduction

The term “Memristor” is a portmanteau from the two words “Memory” and “Resistor”. A memristor (also called a memristive device) typically consists of capacitor-like layer sequences, i.e., a metal-insulator-metal structure. A universal property of the memristive device concept is that the memristive state depends on previously induced charge flows, applied currents, or applied electric fields, which result in different stored resistance states. This simultaneously unique and simple device principle, together with the predicted potential for breakthrough technologies in areas such as universal memories and novel non-Boolean computing schemes for cognitive electronic systems, drives the research and development of memristors and memristor-based circuits. Memristive devices were intensively studied in the last century’s sixties and seventies [1–3]. The field was further driven forward by the establishment of the theoretical background of memristors by Leon Chua (1971), with the corresponding experimental realization and interpretation by the Hewlett-Packard (HP)-Labs (2008) [4, 5].

Currently, two main development avenues can be explored for memristive devices. The first focuses on resistive random access memories (RRAMs). It is believed that the zoo of today’s existing memory diversity can be replaced by a single (universal) memory concept. RRAMs are considered attractive candidates for universal memories because they: show non-volatile data storage, can be densely integrated, are fast, and are cheap to produce. In particular, such a universal memory might attenuate the problem known as memory latency in modern digital computers [6, 7]. Besides the RRAM goal, which may be categorized under the label “More Than Moore”, novel and very appealing computer architectures have been proposed in which memristors might play a vital role. Another main spotlight of possible memristive device applications may be assigned to such catchphrases as non-Boolean computing, bio-inspired information processing, neuromorphic engineering, or cognitive electronics [8–16]. On the local synaptic level, learning in nervous systems is explained by the Hebbian learning rule [17] and, amongst others, spike-timing dependent plasticity (STDP) [18]. STDP and other memory-related mechanisms observed in nervous systems, such as long term potentiation (LTP) and long term depression (LTD) [19], were successfully mimicked by memristive devices [8, 20–22]. To what extent larger networks of memristive devices can mimic higher brain functions is still unknown.

Until now, a huge number of experimental findings on memristor devices consisting of a wide variety of metal/insulator material combinations have been published, all of which show memristive I - V curves [23]. For details concerning resistive switching and the underlying physical-chemical mechanisms, we refer the reader to the overwhelming literature on the subject [12, 14, 23–27]. These physical-chemical mechanisms include electronic effects (e.g., charging of electron traps) [25, 26], magnetic effects (e.g., spin-transfer torque - STT) [28] or ferroelectricity (e.g., ferroelectric tunnel junctions - FTJ) [29]. Moreover, nano-ionic mechanisms are widely utilized to build memristive devices. Included are phase change memory (PCM) devices [30] in which the resistance of the active layer is modulated by switching

Fig. 1 Schematic illustrations of VCM devices based on filament formation (a) and homogeneous ion movement (b)



between crystalline and amorphous phase. Moreover, devices based on the formation and dissolution of conductive filaments composed of metal ions, i.e., the electrochemical metalization effect (ECM) [31], or composed of oxygen vacancies, i.e., the valance change mechanism (VCM) [23, 32], belong to this class. Furthermore, VCM can also be realized without conductive filaments. In these interface-based memristive devices, the resistance is changed by modulating interfacial properties like the Schottky-barrier height [24, 32–34] or the tunneling probability [35–37] by the movement of oxygen vacancies or oxygen ions [23, 25]. Thus, the functionality of VCM devices is based on redox reactions. A sketch of a filamentary-based device and an interface-based device are shown in Fig. 1a and b, respectively. This chapter deals with VCM devices composed of bi-layer metal oxides.

Since the requirements the devices have to fulfill depend on the application, both types of devices are investigated for different purposes, as described in more detail in chapter [Neuromorphic Circuits with Redox-Based Memristive Devices](#) and in further literature [23, 38–41]. In this respect, filamentary-based devices are available in a more mature technology compared to interface-based devices [41]. However, the need for an initial electro-forming step, a current compliance for switching, a pronounced intrinsic randomness of the switching process, and a limited amount of achievable resistance states are some drawbacks compared to interface-based devices [24, 38–42]. On the other hand, endurance, retention, switching speed, and scalability are some of the reported benefits of filamentary devices [38–42]. The properties of interface-based devices will be discussed in further detail in Sect. 2 while the properties of filamentary-based devices are described in Sect. 3.

The quality of the solid-state electrolyte, in which ion movement occurs, determines the switching properties. In this regard, it has been theoretically shown that an oxygen-deficient HfO_x with x between 1.5 and 1.75 is required for the most efficient nucleation of vacancies as the starting point for filament growth [43]. Park et al. [44] experimentally verified this by showing that $x = 1.8$ leads to filamentary switching while $x = 1.98$ leads to interface-based switching. However, stoichiometric HfO_2 matrices are also reported to show filamentary switching enabled through local reduction to HfO_{2-x} [45, 46]. Similar observations are reported for Sr_2TiO_4 [47]. However, in these devices, only the filament-type switching is explained by the

movement of vacancies. In contrast, the interface-based switching is explained by the charging and discharging of electron traps. Moreover, it has been shown that the oxygen content in HfO_x [44, 45] and TaO_x [48] can be used to modify important device parameters in filamentary devices, such as forming and switching voltages, memory window, and high resistance state (HRS) and low resistance state (LRS) currents. Furthermore, adjusting the switching window by tailoring the defect density has also been reported for interface-based devices in simulation studies [44, 49]. Engineering device properties will be discussed in more detail in Sect. 4. The second oxide in the bi-layer system can have different functions, like acting as an oxygen reservoir or a diffusion barrier. A reservoir like TiO_x [50, 51], TaO_x [37], or a TiON formed at a TiN electrode interface [52, 53] allows to increase or decrease oxygen vacancy or ion concentration in the solid-state electrolyte while performing memristive switching. On the other hand, a diffusion barrier like Al_2O_3 [54–57] restricts ion movement within the electrolyte and, thus, can improve retention times [55] or switching linearity [56], and can lead to multi-state operation [56, 57]. It should be noted here that bi-layer metal oxide memristive devices are not necessarily switching by ion migration. As a second switching mechanism, the charging and discharging of electron traps are reported to be responsible for memristive switching in metal oxide junctions [58–63].

Both interface-based and filamentary-based VCM devices consisting of bi-layer metal oxides are described in the following, and exemplary realizations are shown in Sects. 2 and 3, respectively. Strategies to engineer the electrical parameters of these memristive devices to meet the requirements for specific applications are provided in Sect. 4.

2 Interface-Based Devices

The current transport is homogeneously distributed across the electrode area in interface-based memristive devices. Here, the resistance is determined by the interfacial properties of the incorporated materials. Thus, the resistance change is based on altering interfacial properties like Schottky-barrier height or width [24, 32–34] or tunneling probability [35–37]. This is achieved by a rearrangement of oxygen vacancies or oxygen ions [23, 25] or by charging and discharging electron traps [58–60, 62]. In that way, interface-based memristive devices show analog, i.e., gradual switching [24, 35, 41]. Moreover, no electro-forming is needed, and devices with a high I - V non-linearity [33, 64] to avoid the need for additional selector elements for passive crossbar integration [65] are reported. Furthermore, the intrinsic randomness is less pronounced than in filamentary devices [38, 41]. Moreover, interface-based VCM devices have already been integrated into 3D stacks in complementary metal-oxide-semiconductor (CMOS) technology with a minimum feature size of 5 nm [64]. However, CMOS integration and scaling to the nanoscale is challenging for most reported devices [41]. CMOS integration is challenging if the incorporated materials or the needed deposition steps are not used in CMOS fabrication lines or if

the used materials do not withstand the CMOS fabrication steps. This is explained in detail in chapter [Integration of Memristive Devices into a 130 nm CMOS Baseline Technology](#). Downscaling is challenging because the resistance of interface-based devices scales with the electrode area, and most reported devices have high resistances even on the micrometer scale. Drawbacks are, furthermore, a worse retention time and slower switching speed [41] compared to filamentary devices. Therefore, interface-based devices are good candidates to emulate synapses in bio-inspired neuromorphic networks [11, 40], as described in detail in chapter [Neuromorphic Circuits with Redox-Based Memristive Devices](#). Two different devices are described in this section. The first device is based on a $\text{Nb}_x\text{O}_y/\text{Al}_2\text{O}_3$ bi-layer in which Nb_xO_y acts as the solid-state electrolyte while Al_2O_3 is a diffusion barrier restricting ion movement in the Nb_xO_y layer [55]. The second device is based on a $\text{HfO}_2/\text{TiO}_x$ bi-layer. Here, TiO_x acts as an oxygen reservoir, enabling an oxygen exchange with HfO_2 [44].

2.1 Devices Based on $\text{Nb}_x\text{O}_y/\text{Al}_2\text{O}_3$

The first device is named double barrier memristive device (DBMD) [55]. The double oxide layer $\text{Nb}_x\text{O}_y/\text{Al}_2\text{O}_3$ is sandwiched between an Au top electrode and an Nb bottom electrode, as it is sketched in Fig. 2a. The Au leads to a Schottky barrier formation, while alumina acts as a tunnel barrier. The movement of oxygen ions within Nb_xO_y under an applied electric field is reported to be responsible for memristive switching [55, 66], as modeled by a kinetic Monte Carlo simulation [67] which is explained in more detail in chapter [Modeling and Simulation of Silver-Based Filamentary Memristive Devices](#). It should be noted that the charging and discharging of electron traps as the switching mechanism cannot be ruled out [55]. However, a variation in the charge distribution within Nb_xO_y leads to both a variation of the Schottky-barrier height and effective tunneling width. By scaling the solid-state electrolyte down to 2.5 nm, i.e., to the length scale of a single electron wave, the impact of the bulk resistance is minimized, and a very strong mutual interdependency of both barriers is achieved. Thus, both interfaces are altered simultaneously when the charge distribution varies.

Devices with active areas between $70\ \mu\text{m}^2$ and $2500\ \mu\text{m}^2$ are produced on 100 mm Si wafers, which are passivated by a thermal SiO_2 layer. All layers are deposited by DC magnetron sputtering in one and the same vacuum chamber without breaking the vacuum. The devices are structured using standard optical lithography in combination with lift-off and etching steps. Additional passivation with SiO_x enables the deposition of Ti metal contact pads, which allow an automatic measuring of device properties across the whole wafer. This will be discussed in more detail in Sect. 4.1. The fabrication process is explained in detail in [55, 66]. First, Nb and Al are deposited in an Ar atmosphere. The subsequent deposition of Nb_xO_y from a metallic target in an Ar/O₂ atmosphere leads to the fully oxidation of Al to Al_2O_3 , as observed in electron energy loss spectroscopy (EELS) and energy-dispersive X-ray spectroscopy (EDX) in a transmission electron microscope (TEM) [69]. The Nb_xO_y stoichiometry was found to be between the oxidation states Nb_2O_5 and NbO_2 . All

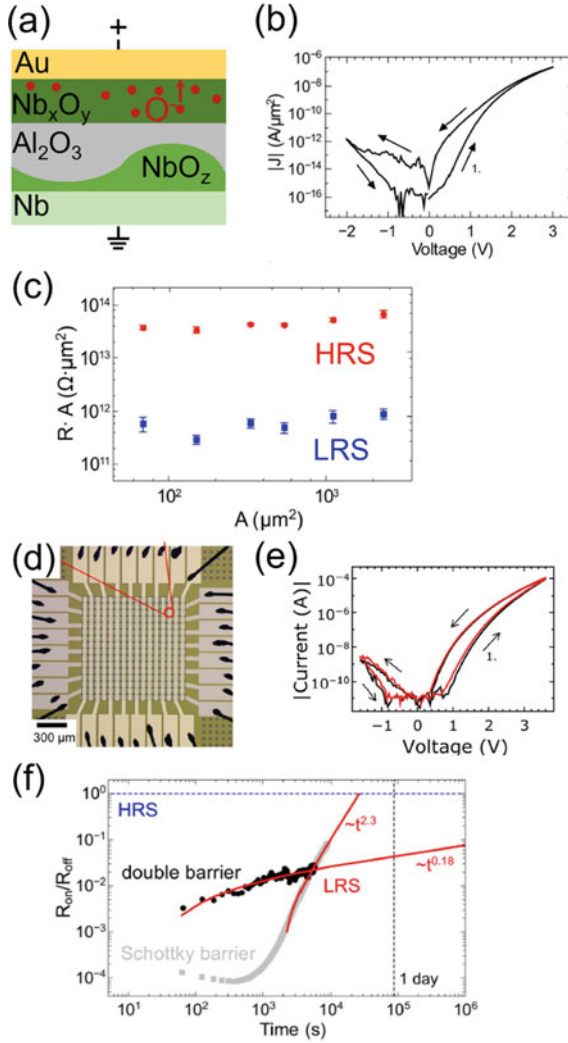


Fig. 2 Double barrier memristive devices (DBMDs). **a** Schematic material stack. **b** Typical $|J|$ - V hysteresis curve. **c** Area-dependent current transport in HRS (red) and LRS (blue). **d** Optical micro-scope photograph of a 16×16 crossbar array containing DBMDs. **e** Typical $|I|$ - V curves of a crossbar-integrated device (red) and a single device (black). **f** Retention of a DBMD (black) and a device without an Al_2O_3 layer. **b**, **f** are reprinted from [55] (licensed under CC BY 4.0), **c** is adapted from [55] (licensed under CC BY 4.0), and **d**, **e** are reprinted from [68] (licensed under CC BY 4.0, <https://creativecommons.org/licenses/by/4.0/>)

interfaces but the Nb/Al₂O₃ interface appeared to be smooth on the nanoscale. Due to the roughness at the lower interface, the thinnest parts of the alumina were determined to be 1.3 nm, as sketched in Fig. 2a. Furthermore, the interface between the Nb bottom electrode and Al₂O₃ was also slightly oxidized. The TEM measurements, including EELS and EDX, are described in more detail in chapter [Critical Discussion of Ex situ and In situ TEM Measurements on Memristive Devices](#).

Figure 2b shows a typical current density versus voltage (J - V) hysteresis curve of a DBMD, which was measured with a grounded Nb electrode, while voltage was applied to the Au electrode. Switching from HRS to LRS is taking place gradually, i.e., in an analog way, by applying a positive voltage to the Au top electrode. Switching back to HRS takes place by applying a negative bias to the top electrode. No initial electro-forming is needed, and an intrinsic current compliance is present. Both HRS and LRS show an area-dependent current transport, as shown in Fig. 2c, since the product of device area A and resistance R results in a constant value for both states. The absolute value of the current density is depicted on a log scale in Fig. 2b, showing the high J - V non-linearity and asymmetry. For dense device integration in a crossbar array, a selector device in series to every memristive element or a strong built-in I - V non-linearity is needed to avoid parasitic currents, i.e., the sneak path problem, when addressing a specific device [65, 70]. The built-in diode-like characteristics of DBMDs allows crossbar integration without needing additional selector devices [68]. A photograph of a crossbar array consisting of 256 DBMDs is shown in Fig. 2d. Here, the devices are located at the cross points of the metallization lines. In that way, each top and bottom contact pad connects the top electrodes in one column of the array. Each left and right pad connects the bottom electrodes of one row. Thus, only 32 contact pads are needed to address all 256 memristive devices. The I - V characteristics of crossbar integrated devices are similar to those of reference devices, as shown in Fig. 2e, in which the black line belongs to a reference device and the red line to a crossbar-integrated device, respectively. Furthermore, Fig. 2f shows the retention time of a DBMD. After the device was set from R_{off} (HRS) to R_{on} (LRS), the resistance was recorded every 60 s with a voltage pulse of 0.5 V amplitude and 2 s duration. In that way, a non-destructive read-out of the resistance state was performed, and the relaxation of the state was measured. The resistance increased fast in the first 600 s (black data points), while afterward, the resistance change was significantly less pronounced. An R_{on}/R_{off} ratio of more than one order of magnitude was still present after one day. This behavior can be quantitatively described by fitting the experimental data to a $\sim t^\beta$ power law (red lines) [61]. In the first 600 s, the relaxation can be described by $\sim t^{0.65}$, while afterward, $\sim t^{0.18}$ holds. That two different power laws are dominant for different time intervals suggests that different physical processes may be responsible for memristive switching, e.g., charging of traps and movement of ions on a faster and slower timescale, respectively. It is also shown in Fig. 2f that the Al₂O₃ considerably affects the retention time. The grey squares show the same measurement on devices without alumina. The retention characteristics of those devices show no resistance increase for the first 700 s but a steep increase afterward fitted by a $\sim t^{2.3}$ power law. Thus, the Al₂O₃ does significantly increase the retention time. Furthermore, the fact that alumina acts as a

diffusion barrier for oxygen [54, 56, 57] is also believed to lead to the self-limited switching behavior due to the limited amount of oxygen ions within Nb_xO_y and no oxygen exchange between both oxides.

The retention time of DBMDs does not allow to use these devices for classical memory applications but for neuromorphic circuits [11]. Bio-inspired learning of visual patterns utilizing crossbar integrated DBMDs as hardware synapses have already been demonstrated [68]. This is explained in chapter [Neuromorphic Circuits with Redox-Based Memristive Devices](#) in detail. However, the drawbacks of DBMDs are those named above for interface-based devices [41]. In this respect, the scalability is challenging due to the high resistance, even on the micrometer scale. For quadratic devices with a feed size of 10 μm , the current in HRS for a typical read-out voltage of 0.5 V is in the pA range. Thus, for scaling the devices down to the nanoscale, the resistance has to be tailored by orders of magnitude. On the other hand, high ohmic devices are desired for low-power applications. Thus, the resistance has to be adjusted so that currents are high enough to be suitable for electronic circuits but low enough to account for energy efficiency. Strategies for engineering device performances are given in Sect. 4. Furthermore, compatibility with CMOS technology is crucial for developing integrated circuits. While Al_2O_3 is a well-known dielectric in CMOS technology, Nb_xO_y in the needed stoichiometry might be more challenging to be integrated into state-of-the-art fabrication lines. Moreover, gold is not desired in CMOS fabrication. Also, the impact of other fabrication steps (e.g., tempering in back-end-of-line processes [71]) has to be considered. CMOS integration of memristive devices is explained in chapter [Integration of Memristive Devices into a 130 nm CMOS Baseline Technology](#). However, if CMOS integration is not possible, devices can be fabricated directly onto CMOS processed substrates in other fabrication lines [72, 73].

After describing device performance, including benefits and drawbacks of the introduced DBMDs, the model for current transport and memristive switching is explained in more detail in the following. Figure 3a shows an equivalent circuit emulating the I - V characteristics [55, 66]. Here, the $\text{Au}/\text{Nb}_x\text{O}_y$ interface is modeled as a Schottky diode D_s , the Nb_xO_y is modeled as a parallel circuit of a resistor R_{NbO} and a capacitor C_{NbO} , and the Al_2O_3 layer is modeled as a voltage-controlled current source I_t emulating elastic tunneling in parallel to a capacitor C_{AlO} . The variable describing the memristive state x denotes the average ion position within the Nb_xO_y . More precisely, thermionic emission theory was employed to model the Schottky diode [74, 75]. According to this theory, charge carriers have enough energy due to an applied electric field to cross the potential barrier between a metal and a semiconductor. For an applied forward bias V , this current can be calculated by

$$I_S = I_R \left(e^{\frac{qV}{nk_B T}} - 1 \right), \quad (1)$$

where q is the elemental charge, k_B is the Boltzmann constant, T is the temperature, and n is the ideality factor. If $n > 1$, deviation from ideal thermionic emis-

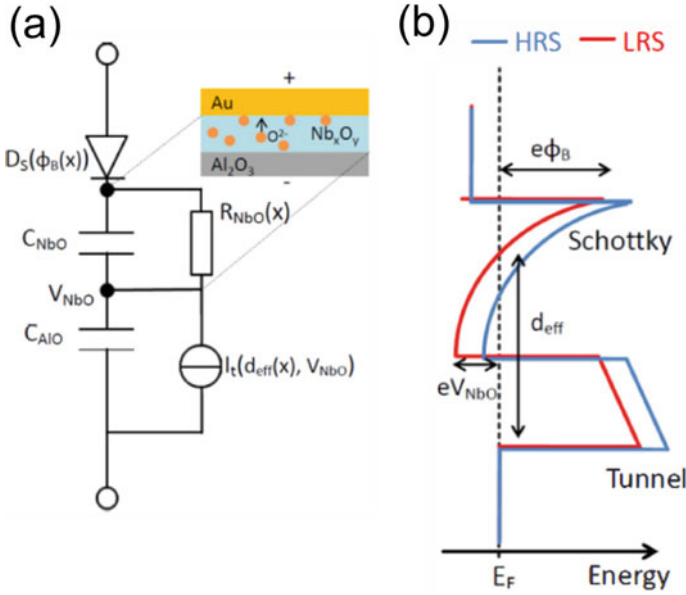


Fig. 3 Model of a DBMD [66] **a** Equivalent circuit **b** Schematic of the band diagram. ©2016 IEEE. Reprinted, with permission, from [M. Hansen et al., IEEE International Conference on Rebooting Computing (ICRC) (2016)]

sion theory is indicated. This deviation can be caused by, e.g., additional tunneling through the barrier (thermionic field emission), additional interface states, or barrier in-homogeneity [74, 75]. The reverse current I_R is given by

$$I_R = A^* A T^2 e^{-\frac{\Phi_B}{k_B T}}. \quad (2)$$

Here, A^* is the effective Richardson constant, A is the device area, and Φ_B is the Schottky barrier height. For reverse bias, however, and if the apparent barrier height Φ_B is reasonably smaller than the band gap of the insulator, the reverse current decreases gradually with the applied negative bias. This can be described by

$$I_{R, V < 0} = -A^* A T^2 e^{-\frac{\Phi_B}{k_B T}} e^{-\frac{\alpha_r \sqrt{|V|}}{k_B T}}. \quad (3)$$

The device-dependent parameter α_r is used to fit the experimentally observed reverse voltage dependency. As it is described in [55], the Schottky diode dominates the current transport for voltages below 0.5 V (LRS) and 1.0 V (HRS). For higher voltages in the forward regime, i.e., higher positive voltages on the Au electrode, the Al_2O_3 tunnel barrier gets relevant and acts as an intrinsic current compliance. The tunneling current can be modeled by the Simmons equation [76]

$$I_{tun} = \frac{KA}{d_{tox}^2} [x_1^2 e^{(-\alpha d_{tox} x_1)} - x_2^2 e^{(-\alpha d_{tox} x_2)}]. \quad (4)$$

In Eq. 4 holds $x_1 = \sqrt{\Phi - eV_I/2}$ and $x_2 = \sqrt{\Phi + eV_I/2}$. Here, Φ is the tunnel barrier height, and V_I is the resulting voltage across the tunnel barrier. Furthermore, A is the device area, K is a constant value, d_{tox} is the barrier thickness, and $\alpha = 2\sqrt{2m}/\hbar$ (m : free electron mass; $\hbar$: Planck's constant divided by 2π).

As it is indicated in Fig. 3a, the Schottky barrier height Φ_B , the effective tunnel barrier width d_{eff} (corresponds to d_{tox} in Eq. 4) as well as the resistance of Nb_xO_y R_{NbO} are dependent on the state variable x , i.e., on the average ion position. Thus, redistribution of oxygen ions within the Nb_xO_y leads to a change in the interfacial properties of the Schottky barrier and the tunnel barrier, while the resistance of Nb_xO_y is only slightly affected [55]. Details about the evolution of x under applied bias and the impact on the interfacial properties can be found in [55, 66]. This model was adapted by Dirkmann et al. [67]. Here, a lumped element circuit model containing the Schottky diode and the tunnel barrier is consistently coupled with a 3D kinetic Monte Carlo model for the ion transport. The simulation results show that the drift of charged oxygen ions within the Nb_xO_y can account for resistive switching behavior. In that way, a Schottky barrier height lowering from 0.90 eV to 0.83 eV, a decrease of the ideality factor from 4.0 to 3.4, and a decrease of the effective tunnel barrier thickness from 1.3 nm to 1.2 nm were determined to explain the R_{on}/R_{off} ratio of more than one order of magnitude. The model also covers the retention behavior. Furthermore, the simulation indicates that the whole applied voltage drops across the Schottky barrier for reverse bias and low forward bias, while the tunnel barrier is responsible for the built-in current compliance at higher forward biases. The model is also described in more detail in chapter [Modeling and Simulation of Silver-Based Filamentary Memristive Devices](#). A sketch of the band diagram for HRS and LRS is given in Fig. 3b and shows the decrease of the Schottky barrier height as well as the tunnel barrier width for switching from HRS to LRS [66].

2.2 Devices Based on HfO_2/TiO_x

Another device based on the oxide bi-layer HfO_2/TiO_x sandwiched between an Au top electrode and a TiN bottom electrode is discussed now [44]. All used materials but the Au are already integrated into CMOS fabrication lines [77]. A typical I - V characteristic for a device with an area of $100 \mu m^2$ is shown in Fig. 4a with grey dots. The switching mechanism is reported to be similar to that of the DBMDs. A Schottky barrier is formed between Au and HfO_2 . Mobile oxygen ions within HfO_2 lead to resistive switching, as sketched in Fig. 4b, c. However, as for the DBMDs, charging and discharging of electron traps cannot be omitted as a reason for switching [44]. The I - V characteristics are qualitatively similar to the DBMDs. Thus, gradual and electro-forming free switching for voltages exceeding a certain threshold and a high I - V non-linearity leading to a diode-like behavior are present.

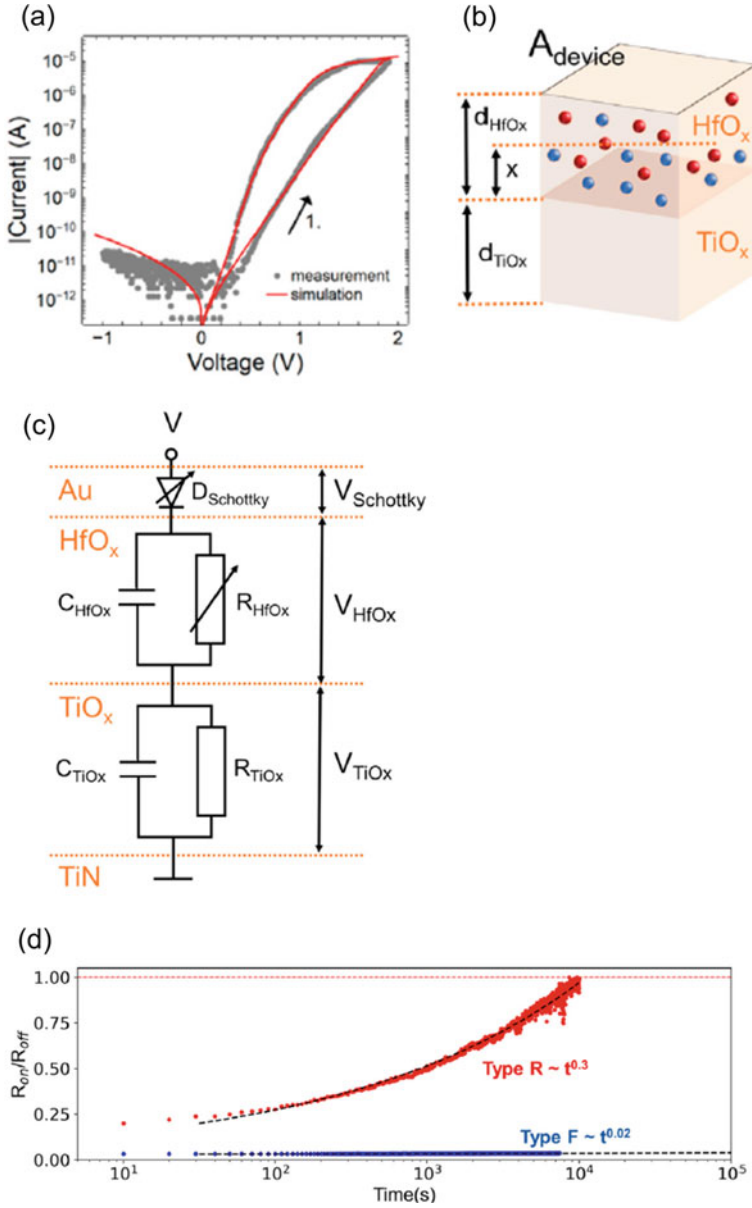


Fig. 4 Interface-based TiN/TiO_x/HfO_x/Au device. **a** Typical $|I|$ - V hysteresis curve. **b** Schematic material stack with indicated switching model. Red and blue spheres indicate mobile oxygen ions and stationary oxygen vacancies, respectively. **c** Equivalent circuit **d** Retention of interface-based devices (red) and filamentary devices (blue). Reprinted from [44] (licensed under CC BY 4.0, <https://creativecommons.org/licenses/by/4.0/>)

However, one difference is that a current compliance of $10\ \mu\text{A}$ is used for switching to prevent dielectric breakdown. Furthermore, the switching window, i.e., the difference between HRS and LRS, decreases with increasing device area. This leads to the fact that the HRS shows an area-dependent current transport while the LRS seems to be not area dependent. However, as it is described in detail in [44], the drift velocity of oxygen ions is modeled to be area dependent, which leads to less switching for increasing device areas and thus to a decreased $R \cdot A$. The retention time can be fitted with a power law function of $\sim t^{0.3}$, depicted in Fig. 4d by the red dots.

The devices are produced with DC magnetron sputtering of all materials without breaking the vacuum and subsequent standard optical lithography and edging steps on 100 mm Si wafers passivated with thermal SiO_2 . Device areas between 100 and $2500\ \mu\text{m}^2$ are fabricated on one and the same wafer. One clear advantage of this material system is that the stoichiometry of HfO_2 can easily be adjusted during sputtering. A $\text{HfO}_{1.98}$, which is named HfO_2 in this chapter for simplicity reasons, leads to the described device performance, while $\text{HfO}_{1.8}$ leads to filamentary-based switching, which is covered by Sects. 3 and 4.2.

The device model shown in Fig. 4c contains a Schottky diode formed between Au and HfO_2 , which is described by thermionic emission theory (see Eqs. 1–3). The oxides are both modeled by parallel RC circuits. The model described in detail in [44] reproduces the I - V characteristics very well, as depicted in Fig. 4a by the red solid line. Here, the resistive switching is dominated by Schottky-barrier height decreasing from 0.71 eV to 0.61 eV and the ideality factor increasing from 3.9 to 4.45 by considering oxygen ion movement as switching mechanism. The model also covers the decreasing $R \cdot A$ with increasing A .

3 Filamentary-Based Devices

Many transition metal oxide-based memristive devices show resistive switching associated with filamentary-type VCM [23, 32, 78]. VCM is triggered by the migration of field-assisted oxygen ion-related defects in transition metal oxides. The oxygen ion-related defects are typically oxygen vacancies that are much more mobile than the transition metal cations [79]. The oxygen vacancy migration and valence change of the cation sub-lattice often appear in the form of the formation and dissolution of a conductive filament in a localized area in the oxide leading to filamentary-type switching.

The resistive switching is typically observed after an initial electro-forming step in filamentary-type devices [79]. Double-positively charged oxygen vacancies (V_0^{++}) are generated by electro-forming, and the V_0^{++} s migrate under the applied electric field. If V_0^{++} s are close to each other, a single charged state (V_0^+) becomes more favorable. The cluster of V_0^+ s are arranged in a filament structure, where the V_0^+ has a significantly higher energy barrier for diffusion than V_0^{++} [80]. The localized conductive filament leads to reversible changes of local resistivity and overall device resistance [81]. The vacancies located in the filament have a high diffusion

energy barrier. Therefore, the filamentary-type devices typically show long retention properties.

The bi-layer metal oxide devices typically consist of an oxygen vacancy reservoir layer and a solid-state electrolyte layer for filamentary-type memristive devices [82]. Under an applied electric field, oxygen vacancies are injected into the solid-state electrolyte from the reservoir layer. The oxygen vacancies form a localized conductive filament in the electrolyte layer, which reduces the overall resistance. If the electrolyte layer builds a Schottky-like barrier at the interface to the contacting metallic electrode, the conductive filament leads to a lowering of the barrier height and, thus, the overall device resistance [50]. The filamentary devices can be recognized by the resistance-area product [83]. The resistance in the ON state (LRS) is independent of the electrode area size because the conductive filament is created in a localized form.

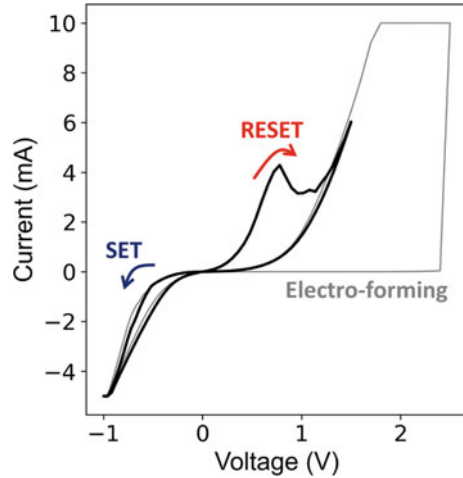
The benefits of filamentary RRAM devices are manifold. These devices can show a high endurance, high retention time, a fast switching speed (up to ns regime), and great scalability in the nm regime [38–42]. Moreover, they have already been integrated into CMOS technology, allowing to combine traditional electronic circuits with RRAM devices on the very same chip [77, 84–87], and even 3D integration has been shown [84, 88, 89]. Drawbacks are the need for an initial electro-forming step and a current compliance for switching, the need for selector devices to integrate them in memory arrays, pronounced intrinsic randomness of the switching process, a limited amount of achievable resistance states, and a rather low resistance [38–42, 65, 70]. However, a bi-layer metal oxide concept has recently attracted attention to tackle the intrinsic randomness issue in filamentary devices [57]. Besides, randomness can be exploited for certain tasks [90, 91]. Moreover, even though most RRAM devices can only be switched between two resistance states (binary devices), multilevel devices have already been reported. For this multi-state operation, a variable current compliance for switching to LRS and a variable switching voltage for switching to HRS are usually needed [45, 52, 92–94], or variable pulse widths can be used [45]. However, devices showing a gradual switching with identical pulses have also been reported [56, 95]. Moreover, more sophisticated programming algorithms are reported to reach specific resistive states [57, 85, 87, 88, 94, 96, 97].

In this section, a $\text{TiO}_x\text{-HfO}_x$ bi-layer oxide device is mainly presented as an example of a filamentary-based VCM memristive device [44]. Using the $\text{TiO}_x\text{-HfO}_x$ bi-layer oxide device, typical electrical characteristics of filamentary-based devices are shown.

The $\text{TiO}_x\text{-HfO}_x$ memristive devices consist of TiN (50 nm) as the bottom electrode, TiO_x (30 nm)/ HfO_x (2–8 nm) metal oxide bi-layers, and Au (50 nm) as the top electrode. The devices were fabricated on a 4-inch wafer, where the devices have 6 different active area sizes with a thickness gradient of the HfO_x layer from 2 nm to 8 nm. This 4-inch wafer fabrication process enables to exclude wafer-to-wafer variability, and study the effect of the area size and the thickness of HfO_x on the electrical properties of the memristive devices.

In Fig. 5, the $\text{TiO}_x\text{-HfO}_x$ bi-layer memristive devices show a typical I - V curve as a filamentary-type device. At first, an electro-forming step was required to initiate the

Fig. 5 I - V curve obtained by DC voltage sweep measurement showing RS and electro-forming in the filamentary $\text{TiO}_x/\text{HfO}_x$ devices



resistive switching in the $\text{TiO}_x/\text{HfO}_x$ memristive device. The electro-forming process was characterized by an abrupt jump in the current at a higher voltage (2.3 V) than the SET/RESET voltages. However, a high voltage through electro-forming could make it difficult for memristive devices to be integrated into CMOS circuits. Strategies to overcome this issue are already reported [45, 98, 99] and are addressed in Sect. 4.2.

After the electro-forming cycle, the resistive switching is observed in the $\text{TiO}_x/\text{HfO}_x$ memristive device. The switching required external current compliance of 5 mA for the SET process, while the RESET exhibited a compliance-free behavior. Bipolar switching properties were observed, and the amplitudes of switching voltages were symmetric, with -0.7 V and 0.7 V for SET and RESET, respectively. The $\text{TiO}_x/\text{HfO}_x$ device featured gradual switching characteristics, while typical filamentary type devices show an abrupt SET process. The origin of the abrupt transition during SET is related to positive feedback between the current increase and Joule heating [100]. In order to achieve a gradual switching behavior, a layer stack modification [100] and a multi-layer stack approach [51] have been proposed. In the multi-layer stack concept, for example, the $\text{TiO}_x/\text{HfO}_x$ bi-layer oxide can be exploited, where TiO_x serves as a reservoir for oxygen vacancies and stabilizes the switching process [57]. A gradual switching can promote uniformity during device operation. Furthermore, a gradual resistance transition during both SET and RESET is favorable for analog computing applications [101].

Gradual switching is often related to analog behavior. The analog behavior can be investigated using pulse measurements, applying a train of voltage pulses to memristive devices. Figure 6a shows the switching behaviors of the $\text{TiO}_x/\text{HfO}_x$ device in a pulse measurement. For the measurement, 20 SET voltage pulses followed by 20 RESET voltage pulses are applied, while a reading pulse is applied after each switching pulse to read the resistance of the device. The $\text{TiO}_x/\text{HfO}_x$ device shows a non-linear transition from the SET to the RESET, as shown in Fig. 6a. However,

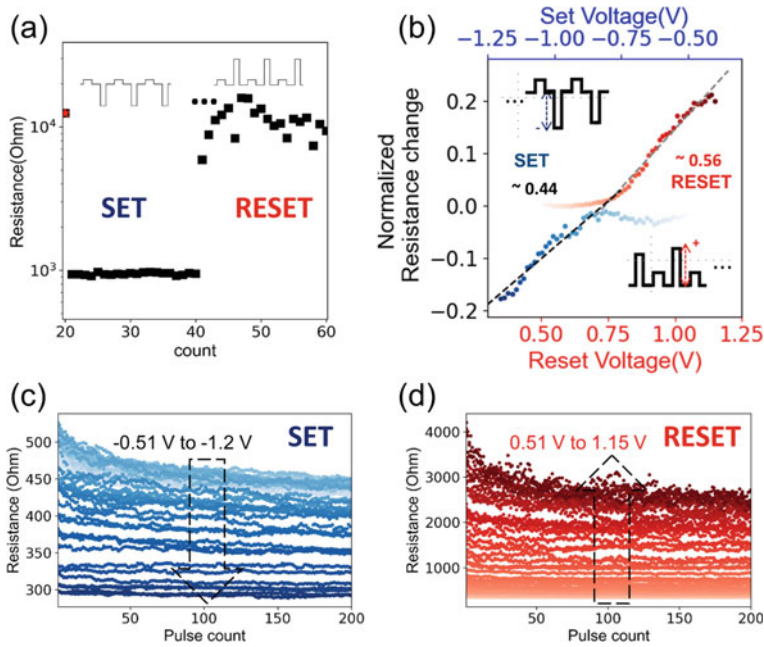


Fig. 6 **a** A train of 20 set voltage pulses and the subsequent 20 reset voltage pulses. A non-linear transition from the SET to the RESET is observed. **b** Linear trend in the resistance change in dependency on the amplitude of the switching pulse voltage. **c** Multi-state in the SET and **d** in the RESET resulting from the adjusted amplitude of switching voltages. **b** is reproduced from [44] (licensed under CC BY 4.0, <https://creativecommons.org/licenses/by/4.0/>)

the magnitude of resistance change is influenced by the amplitude of the applied switching voltage pulses in Fig. 6c, d. The impact of pulse amplitude is observed by applying switching voltage pulses with varied amplitude, each followed by 200 reading pulses. Furthermore, the median values of resistance were extracted from Fig. 6c, d, and the resistance change from the initial state was calculated at each switching voltage amplitude. The resistance change showed symmetry in Fig. 6b between the SET and the RESET operation. Symmetric and analog resistive switching is desirable for neuromorphic computing since this makes the programming of the memristive device more efficient [102].

Another indication of the filamentary-type device can be the retention property. In Fig. 4d, the retention property of the $\text{TiO}_x/\text{HfO}_x$ device is compared to the interface-type device described in Sect. 2. The interface-type device has the same material configuration but fewer oxygen vacancies in the HfO_x layer ($x = 1.98$). The filamentary-type device shows a much longer retention time than the interface-type device due to the high diffusion barrier of the vacancies within the filament. This has been quantitatively shown by fitting the retention measurement to the $\sim t^\beta$ power law [61] introduced in Sect. 2, leading to $\beta = 0.02$ compared to $\beta = 0.3$ for the

interface-based devices. Thus, the relaxation of the resistance is proceeding orders of magnitude slower in the filamentary devices.

4 Engineering *I-V* Characteristics of Memristive Devices

The possibility of adapting electrical parameters of memristive devices allows engineering the device performance to meet the requirements for specific applications [45, 49]. Parameters such as switching voltage, forming voltage, HRS, LRS, the switching dynamics, or the number of resistance states can be engineered. Typical strategies are tailoring the switching oxide itself by adjusting the stoichiometry or the density of oxygen vacancies or ions [44, 45, 47–49], doping with additional cations [94], or using different oxide phases [91, 94]. Furthermore, adding additional oxide layers to affect the oxygen exchange [55–57] or the local temperature distribution [51] can impact the memristive behavior. Geometrical parameters like the switching oxide thickness [44, 71] or the device area [44, 55] can also influence the *I-V* characteristics. In Sect. 4.1, strategies for tailoring the interface-based devices introduced in Sect. 2 are described. This includes a thorough analysis of the process plasma during sputter deposition of DBMDs. Section 4.2 deals with engineering approaches to tailor the filament-based devices shown in Sect. 3.

4.1 Engineering of Interface-Based Devices

The devices described in Sect. 2 are fabricated by magnetron sputtering [103, 104]. The thin film deposition conditions like pressure, gas composition, structure and strength of the magnetic field, amplitude and form of discharge, and substrate position and orientation strongly influence electrical and optical material properties [105–109]. In this respect, gas flow rates and the resulting pressure significantly impact particle energies and, thereby, the structure and density of deposited films [106, 107]. Furthermore, the gas composition affects chemical reactions in the gas phase and at surfaces (target, substrate), influencing, e.g., the stoichiometry. Moreover, the substrate position and orientation relative to the sputter target affect film properties since particle fluxes and electric potentials in the plasma environment can show strong spatial in-homogeneity due to, e.g., structure and strength of the involved magnetic field [105, 107–109]. Another crucial parameter during reactive sputter deposition in an electronegative gas like O_2 is the density of negatively charged ions. If the target surface gets completely poisoned, negative oxygen ions are formed and accelerated by the electric field towards the substrate. This can cause defects or stress in deposited materials due to the high kinetic energy [105, 110]. The radial distribution, the energy, and the impinging angle of these ions depend on the erosion of the target (i.e., the target geometry) and the discharge voltage. It has been shown that the erosion state of a target can be correlated with the resistivity of oxides,

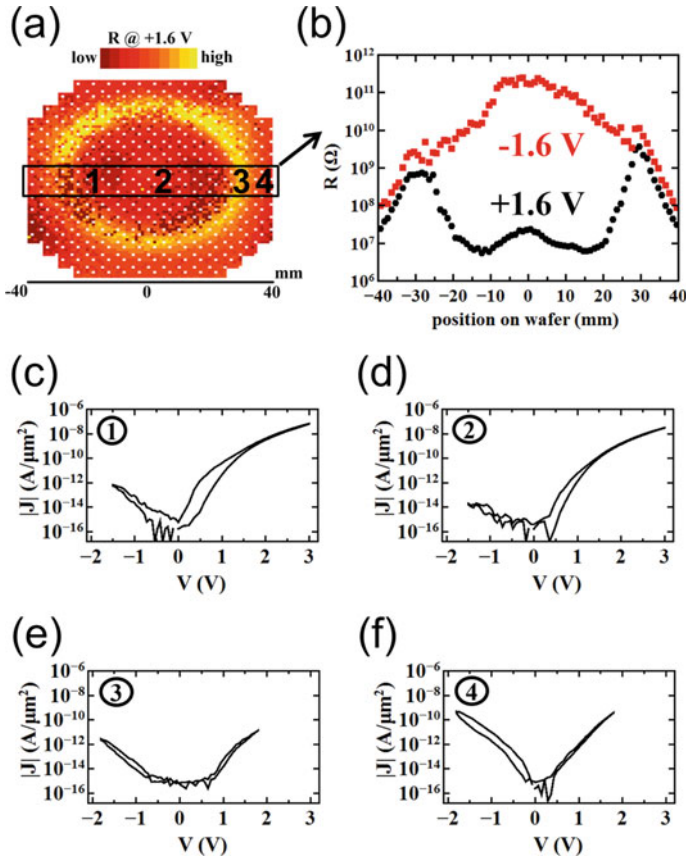


Fig. 7 Electrical characterization of DBMDs at different positions on a 100 mm wafer: **a** Resistance map measured with 1.6 V. **b** Device resistance dependent on radial position for positive bias (black dots) and negative bias (red squares). **c–f** Typical $|J|$ - V curves at different radial positions 1 to 4 (–25 mm, +5 mm, +30 mm, and +35 mm). Reprinted from [49] [F. Zahari et al., Journal of Vacuum Science & Technology B 37, 061203 (2019)], with the permission of AIP Publishing

attributed to the impact of negatively charged oxygen ions [105, 111]. The erosion is almost only taking place in a ring-shaped area (called race track) determined by the magnetic field.

To correlate the plasma properties to the electrical characteristics of DBMDs, several plasma parameters of the Nb_xO_y deposition process were measured at different positions underneath the Nb target since the I - V characteristics vary at different positions on the 100 mm wafer [49]. Figure 7 shows the device-to-device variation across the whole wafer. Figure 7a contains a resistance map measured with read-out voltages of 1.6 V on a spatial resolution of 1 mm, showing circular symmetry. Here, 5336 devices with an area of $400 \mu\text{m}^2$ were measured. Figure 7b depicts the dependence of the resistance for positive (black dots) and negative (red squares) bias on the radial position. Therefore, the resistances of up to ten devices

were averaged for each position. Defective devices (short-circuited or not properly connected to the wiring) and test structures [gray squares in Fig. 7a] were not used for averaging. In the inner area of the wafer with a radius of about 25 mm, current rectification is observed, and the devices show memristive behavior as described in Sect. 2. However, not only the resistance but also the switching window varies with position, as can be seen by comparing Fig. 7c with d. The yellow ring in Fig. 7a, starting at about 30 mm away from the center, contains devices with relatively high resistance. The I - V characteristics differ significantly from the functional devices in the center [Fig. 7e]. No rectification and no hysteresis can be observed. Here, the race track of the target is located. In the outer red area in Fig. 7a, the resistance is rather low and comparable to the resistance in the inner area. However, no rectification and no hysteresis are apparent [Fig. 7f]. It should be noted that I - V curves with lower voltages are depicted in Fig. 7e, f because the devices suffer dielectric breakdown for higher voltages at these locations.

As described above, devices located at different positions on a 100 mm wafer show significant different I - V characteristics even though they were produced in one and the same process. Thus, the DBMDs are well suited to correlate plasma process parameters with material properties and, finally, with electrical properties [49]. The overall goal is first to understand the impact of several plasma parameters on the electrical properties and second to use these findings to develop a process to fabricate plasma-engineered devices tailored for specific applications. Thus, plasma parameters were recorded with a probe consisting of a sensor copper plate (11 mm in diameter) connected at the backside to a thermocouple for temperature measurement ($40 \mu\text{V/K}$) and a copper bias wire [109]. This was used as a passive thermal probe (PTP) [109, 112] and as a Langmuir probe (LP) [113, 114]. A PTP is used to measure the energy balance at the location of the sample. The energy flux is dominated by impinging particles, surface reactions, incoming radiation, and loss processes such as heat conduction and convection through the surrounding gas and by emitted radiation [106]. Therefore, the energy balance depends on the process parameters named above, and it has a crucial impact on film properties [106, 107, 115]. The energy balance during Nb_xO_y deposition at different positions is shown in Fig. 8a. With an LP, on the other hand, additional process parameters like the electron temperature T_e [Fig. 8b], the floating potential of the probe Φ_{fl} [Fig. 8c], the plasma potential Φ_{pl} [Fig. 8d], and the current density of positively charged ions to the probe j_{ion} [Fig. 8e] are measured by applying a voltage sweep to the bias wire and evaluating the measured current [116, 117]. While the energy flux and j_{ion} show a Gaussian distribution with maxima in the center as expected for an unbalanced magnetron, the other parameters show a more complex dependency on the position. In particular, T_e and Φ_{pl} have local maxima at the location of the race track, while Φ_{fl} has local minima approx. 20 mm away from the center, where the devices show the largest switching window and the lowest resistance for positive bias together with a pronounced rectification [compare Fig. 7a–d]. Thus, it is expected that the effect of the energy balance superimposes with the other plasma parameters and with the distribution of negatively charged oxygen ions to obtain a Nb_xO_y film having properties (e.g., oxidation state and defect concentrations) as needed for memristive switch-

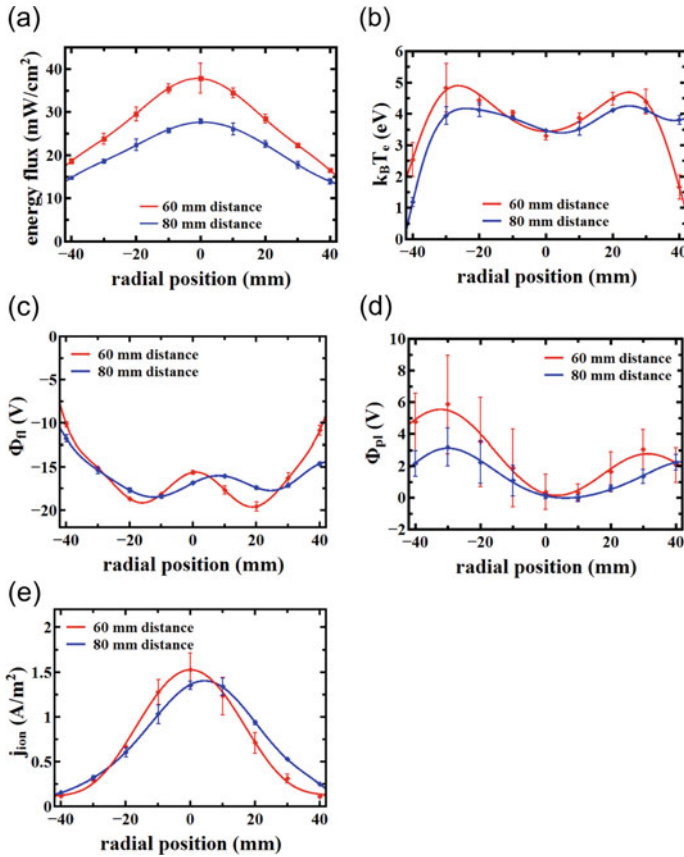


Fig. 8 Plasma parameters in dependency on the radial position. **a** Energy flux **b** Electron temperature, **c** Floating potential of probe **d** Plasma potential **e** Current of positive ions. In **a–e**, the mean values and the standard deviations determined with two measurements for each position (three for the center position) are depicted (squares with error bars). The solid and dashed lines show fits of the mean values. Results obtained with a target to probe distance of 60 mm and 80 mm are shown in red (squares/solid lines) and blue (squares/dashed lines), respectively. Reprinted from [49] [F. Zahari et al., Journal of Vacuum Science & Technology B 37, 061203 (2019)], with the permission of AIP Publishing

ing in DBMDs. This knowledge can potentially be exploited for engineering device performance by using multiple frequency capacitively coupled plasmas (MFCCPs) for sputter deposition. An MFCCP allows to control the ion energy and the ion flux independently of one another during sputtering and thus can help to control different process parameters [118, 119].

To show the influence of the plasma parameters on the stoichiometry of Nb_xO_y , TEM/EELS measurements were performed on two different devices, one located at a radial position of 5 mm (showing memristive behavior) and one at a radial position of -30 mm (showing relatively high resistance and no switching), respectively [49].

While Nb_xO_y of the functional device is in a high oxidation state between Nb_2O_5 and NbO_2 , as already shown before [69], the Nb_xO_y from the non-functional device shows significantly less incorporated oxygen and cannot be assigned to one of the known niobium oxidation states (i.e., Nb_2O_5 , NbO_2 , or NbO). Furthermore, the film thickness does vary only by 0.1 nm between both positions and thus within the standard deviation of the TEM measurement. The deviation in film thickness does not explain the substantial deviation in I - V characteristics since devices with both thicknesses lead to memristive switching devices if they are located within the center of the wafer. Thus, the deviations of the I - V characteristics can be mainly attributed to the chemical and electronic properties of the niobia, while the geometrical properties are less important. This can indeed be correlated to the plasma process parameters. Moreover, the kinetic Monte Carlo simulations [67] introduced in Sect. 2 were extended to show the impact of the concentration of the mobile charged defects on the switching window [49]. The results are depicted in Fig. 9a. In particular, it is shown that an increase in defect concentration n_d from $2 \cdot 10^{20} \text{ cm}^{-3}$ to $8 \cdot 10^{20} \text{ cm}^{-3}$ increases the switching window at 0.5 V from a factor of approx. 3 to a factor of approx. $4 \cdot 10^5$. Thus, increasing the defect concentration by a factor of 4 does lead to an increased switching window by five orders of magnitude. Increasing ion concentration in the interface-based $\text{HfO}_x/\text{TiO}_x$ device also leads to a larger switching window shown by simulations [44]. Furthermore, as it is shown in Fig. 9b, also the voltage range in which a hysteresis loop can be observed changes with ion concentration, and the reverse current is also more affected as in the model of the DBMDs.

4.2 Engineering of Filamentary-Based Devices

This section presents methodologies to engineer the characteristics of the filamentary-type memristive devices, such as electro-forming, I - V non-linearity, retention, and variability. In particular, engineering methods for the $\text{TiO}_x/\text{HfO}_x$ memristive devices, that are presented in Sect. 3, are further described.

The concentration of oxygen vacancies in the metal oxide is one of the decisive parameters for the filamentary-type switching behaviors [43]. In the $\text{TiO}_x/\text{HfO}_x$ memristive device, the HfO_x showed a substoichiometric property of $x = 1.8$ in X-ray photoelectron spectroscopy (XPS) measurements. The HfO_x layer had an optimal environment for efficient electro-forming and filamentary-type switching [43]. In the $\text{TiO}_x/\text{HfO}_x$ devices, oxygen deficiency in the HfO_x was achieved by deliberately growing a substoichiometric oxide film using a wedge sputtering method. Another approach to modifying the oxygen vacancies in the oxide layer is inserting an oxygen scavenging metal layer [120]. As already stated above, adjusting the vacancy concentration is a common way to adjust electrical switching parameters like forming voltage or switching voltages [45, 48, 98, 99]. Another method for scaling the forming voltage is tuning the thickness of the metal oxide layer. In Fig. 10, the electro-forming voltage in the $\text{TiO}_x/\text{HfO}_x$ device showed a dependency on the thickness of

Fig. 9 Modeled hysteresis curves dependent on the mobile defect concentration.

a $|J|$ - V curves of DBMDs.

Reprinted from [49] [F.

Zahari et al., Journal of

Vacuum Science &

Technology B 37, 061203

(2019)], with the permission

of AIP Publishing. **b** $|I|$ - V

curves of interface-based

TiN/TiO_x/HfO_x/Au device.

Reprinted from [44]

(licensed under CC BY 4.0,

[https://creativecommons.org/](https://creativecommons.org/licenses/by/4.0/)

<https://creativecommons.org/licenses/by/4.0/>)

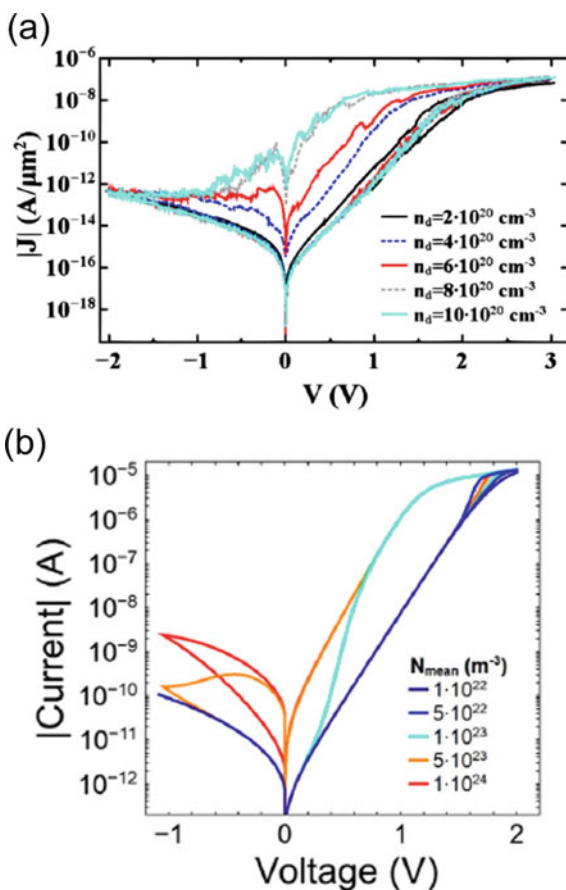
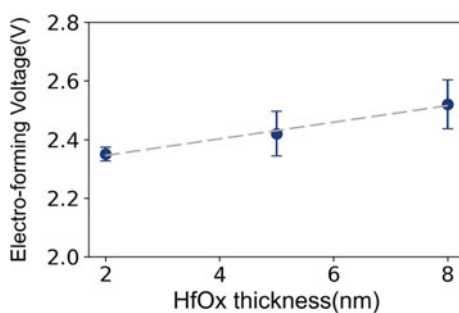


Fig. 10 Tailoring of the electro-forming voltage in the filamentary TiO_x/HfO_x devices by tuning the HfO_x thickness. Reprinted from [44] (licensed under CC BY 4.0,

[https://creativecommons.org/](https://creativecommons.org/licenses/by/4.0/)

<https://creativecommons.org/licenses/by/4.0/>)



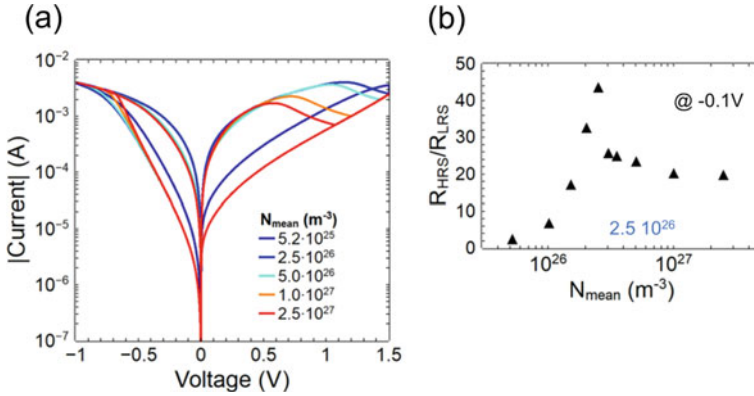
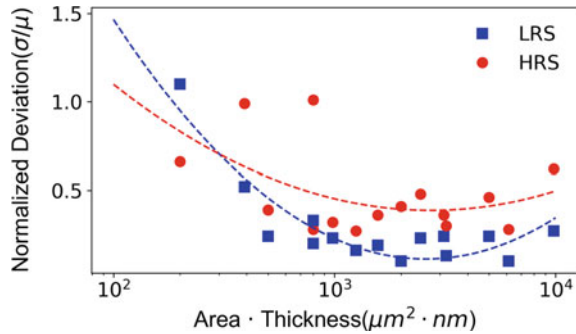


Fig. 11 Impact of the oxygen vacancy concentration on the switching hysteresis determined by simulations. Reprinted from [44] (licensed under CC BY 4.0, <https://creativecommons.org/licenses/by/4.0/>). **a** Concentration of oxygen vacancies and resistive switching behavior. **b** Switching window as a function of the concentration of the oxygen vacancies

Fig. 12 $\text{TiO}_x/\text{HfO}_x$ device variability dependent on the product of the active area and the HfO_x thickness. Reprinted from [44] (licensed under CC BY 4.0, <https://creativecommons.org/licenses/by/4.0/>)



the HfO_x . The thicker the switching oxide layer, the higher the voltage required to initiate resistive switching.

Besides impacting forming and switching voltages, the vacancy concentration also affects the switching hysteresis. In Fig. 11a, the simulation result shows such an impact on the $\text{TiO}_x/\text{HfO}_x$ device. There is an optimum concentration of oxygen vacancies at $2.5 \cdot 10^{26} \text{ m}^{-3}$, where the $\text{TiO}_x/\text{HfO}_x$ device has the maximum switching window at a read-out voltage of -0.1 V , shown in Fig. 11b. The simulation shows that the device suffers from a higher concentration of oxygen vacancies due to the threshold value of oxygen diffusion [44].

Formation and dissolution of filaments are stochastic processes, which means the filamentary-type devices typically show a high variability during the switching. However, scaling the active area size down can reduce the variability [120]. Moreover, the study of the $\text{TiO}_x/\text{HfO}_x$ filamentary devices shows that the variability can be influenced by the correlation between the thickness of the oxide layer and the active

area size. As shown in Fig. 12, an optimal combination of the oxide thickness and the active area size exists to obtain reliable switching operation.

The comparison of the retention time of interface-based and filamentary-type $\text{TiO}_x/\text{HfO}_x$ devices [see Fig. 4d] implies that the modification of oxygen deficiency in the HfO_x layer can control the retention property. In this respect, many studies show methods to enhance the retention time by introducing retention stabilization layers to modify the oxygen deficiency [54, 121].

Acknowledgements Funded by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) - Project-ID 434434223 - SFB 1461. Moreover, the financial support by the DFG via the Research Unit 2093 is acknowledged.

References

1. Hickmott, T.W.: Low-frequency negative resistance in thin anodic oxide films. *J. Appl. Phys.* **33**, 2669–2682 (1962)
2. Argall, F.: Switching phenomena in titanium oxide thin films. *Solid-State Electron.* **11**, 535–541 (1968)
3. Dearnaley, G., Stoneham, A.M., Morgan, D.V.: Electrical phenomena in amorphous oxide films. *Rep. Prog. Phys.* **33**, 1129–1191 (1970)
4. Chua, L.: Memristor-the missing circuit element. *IEEE Trans. Circuit Theory* **18**, 507–519 (1971)
5. Strukov, D.B., Snider, G.S., Stewart, D.R., et al.: The missing memristor found. *Nature* **453**, 80–83 (2008)
6. Iniewski, K. (ed.): *CMOS Processors and Memories*. Springer Netherlands (2010). ISBN: 978-90-481-9215-1. <https://doi.org/10.1007/978-90-481-9216-8>
7. Banerjee, W.: Challenges and applications of emerging nonvolatile memory devices. *Electronics* **9**, 1029 (2020)
8. Linares-Barranco, B., Serrano-Gotarredona, T., Camu-as-Mesa, L., et al.: On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex. *Front. Neurosci.* **5**, 26 (2011)
9. Ranjan, R., Ponce, P.M., Hellweg, W.L., et al.: Integrated circuit with memristor emulator array and neuron circuits for biologically inspired neuromorphic pattern recognition. *J. Circuit Syst. Comp.* **26**, 1750183 (2017)
10. Hu, M., Graves Catherine, E., Li, C., et al.: Memristor-based analog computation and neural network classification with a dot product engine. *Adv. Mater.* **30**, 1705914 (2018)
11. Ziegler, M., Wenger, C., Chicca, E., et al.: Tutorial: concepts for closely mimicking biological learning with memristive devices: principles to emulate cellular forms of learning. *J. Appl. Phys.* **124**, 152003 (2018)
12. Wang, R., Yang, J.-Q., Mao, J.-Y., et al.: Recent advances of volatile memristors: devices, mechanisms, and applications. *Adv. Intell. Syst.* **2**, 2000055 (2020)
13. Spiga, S., Sebastian, A., Querlioz, D., et al.: *Memristive Devices for Brain-Inspired Computing: From Materials, Devices, and Circuits to Applications - Computational Memory, Deep Learning, and Spiking Neural Networks*. Woodhead Publishing (2020). ISBN: 978-0-08-102787-5
14. Bian, H., Goh, Y.Y., Liu, Y., et al.: Stimuli-responsive memristive materials for artificial synapses and neuromorphic computing. *Adv. Mater.* **33**, 2006469 (2021)
15. Sun, K., Chen, J., Yan, X.: The future of memristors: materials engineering and neural networks. *Adv. Funct. Mater.* **31**, 2006773 (2021)

16. Kaspar, C., Ravoo, B.J., van der Wiel, W.G., et al.: The rise of intelligent matter. *Nature* **594**, 345–355 (2021)
17. Hebb, D.O.: *The Organization of Behavior: A Neuropsychological Theory*. Psychology Press, New York (2002). ISBN: 978-1-4106-1240-3. <https://doi.org/10.4324/9781410612403>
18. Bi, G.-Q., Poo, M.-M.: Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type. *J. Neurosci.* **18**, 10464–10472 (1998)
19. Bliss, T.V.P., Lømo, T.: Long-lasting potentiation of synaptic transmission in the dentate area of the anaesthetized rabbit following stimulation of the perforant path. *J. Physiol.* **232**, 331–356 (1973)
20. Jo, S.H., Chang, T., Ebong, I., et al.: Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **10**, 1297–1301 (2010)
21. Ohno, T., Hasegawa, T., Tsuruoka, T., et al.: Short-term plasticity and long-term potentiation mimicked in single inorganic synapses. *Nat. Mater* **10**, 591–595 (2011)
22. Winterfeld, H., Ziegler, M., Hanssen, H., et al.: Technology and electrical characterization of memflash cells for neuromorphic applications. *J. Phys. D: Appl. Phys.* **51**, 324003 (2018)
23. Ielmini, D., Waser, R. (eds.): *Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications*. Wiley-VCH Verlag GmbH & Co., KGaA, Weinheim (2016). ISBN: 978-3- 527-33417-9
24. Sawa, A.: Resistive switching in transition metal oxides. *Mater. Today* **11**, 28–36 (2008)
25. Waser, R., Dittmann, R., Menzel, S., et al.: Introduction to new memory paradigms: memristive phenomena and neuromorphic applications. *Faraday Discuss.* **213**, 11–27 (2019)
26. Wang, J., Zhuge, X., Zhuge, F.: Hybrid oxide brain-inspired neuromorphic devices for hardware implementation of artificial intelligence. *Sci. Technol. Adv. Mater.* **22**, 326–344 (2021)
27. Lanza, M., Waser, R., Ielmini, D., et al.: Standards for the characterization of endurance in resistive switching devices. *ACS Nano* **15**, 17214–17231 (2021)
28. Kawahara, T., Ito, K., Takemura, R., et al.: Spin-transfer torque RAM technology: review and prospect. *Microelectron. Reliab.* **52**, 613–627 (2012)
29. Garcia, V., Bibes, M.: Ferroelectric tunnel junctions for information storage and processing. *Nat. Commun.* **5**, 4289 (2014)
30. Burr, G.W., Brightsky, M.J., Sebastian, A., et al.: Recent progress in phase-change memory technology. *IEEE J. Emerg. Sel. Top. Circuits Syst.* **6**, 146–162 (2016)
31. Valov, I., Waser, R., Jameson, J.R., et al.: Electrochemical metallization memories-fundamentals, applications, prospects. *Nanotechnology* **22**, 254003 (2011)
32. Waser, R., Dittmann, R., Staikov, G., et al.: Redox-based resistive switching memories - nanoionic mechanisms, prospects, and challenges. *Adv. Mater.* **21**, 2632–2663 (2009)
33. Park, S., Jung, S., Siddik, M., et al.: Self-formed schottky barrier induced selector-less rram for cross-point memory applications. *Physica status solidi (RRL) – Rapid Res. Lett.* **6**, 454–456 (2012)
34. Hsu, C.-W., Wang, Y.-F., Wan, C.-C., et al.: Homogeneous barrier modulation of TaO_x/TiO₂ bilayers for ultra-high endurance three-dimensional storage-class memory. *Nanotechnology* **25**, 165202 (2014)
35. Meyer, R., Schloss, L., Brewer, J., et al.: Oxide dual-layer memory element for scalable non-volatile cross-point memory technology. In: 2008 9th Annual Non-Volatile Memory Technology Symposium (NVMTS), pp. 1–5 (2008). <https://doi.org/10.1109/NVMT.2008.4731194>
36. Govoreanu, B., Redolfi, A., Zhang, L., et al.: Vacancy-modulated conductive oxide resistive ram (vmco-rram): an area-scalable switching current, self-compliant, highly nonlinear and wide on/off-window resistive switching cell. In: 2013 IEEE International Electron Devices Meeting, pp. 10.2.1–10.2.4 (2013). <https://doi.org/10.1109/IEDM.2013.6724599>
37. Baeumer, C., Heisig, T., Arndt, B., et al.: Spectroscopic elucidation of ionic motion processes in tunnel oxide-based memristive devices. *Faraday Discuss.* **213**, 215–230 (2019)
38. Burr, G.W., Shelby, R.M., Sebastian, A., et al.: Neuromorphic computing using non-volatile memory. *Adv. Phys. X* **2**, 89–124 (2017)

39. Ielmini, D., Wong, H.-S.P.: In-memory computing with resistive switching devices. *Nat. Electron* **1**, 333–343 (2018)
40. Sebastian, A., Le Gallo, M., Khaddam-Aljameh, R., et al.: Memory devices and applications for in-memory computing. *Nat. Nanotechnol.* **15**, 529–544 (2020)
41. Christensen, D.V., Dittmann, R., Linares-Barranco, B., et al.: 2022 Roadmap on Neuromorphic Computing and Engineering (2021). [arXiv:2105.05956](https://arxiv.org/abs/2105.05956) [cond-mat]
42. Wong, H.S.P., Lee, H.Y., Yu, S., et al.: Metal-oxide RRAM. *Proc. IEEE* **100**, 1951–1970 (2012)
43. McKenna, K.P.: Optimal stoichiometry for nucleation and growth of conductive filaments in HfO_x . *Modell. Simul. Mater. Sci. Eng.* **22**, 025001 (2014)
44. Park, S., Klett, S., Ivanov, T., et al.: Engineering method for tailoring electrical characteristics in TiN/TiOx/HfOx/Au bi-layer oxide memristive devices **3**, 16 (2021)
45. He, W., Sun, H., Zhou, Y., et al.: Customized binary and multi-level HfO_{2-x} -based memristors tuned by oxidation conditions. *Sci. Rep.* **7**, 10070 (2017)
46. Sokolov, A.S., Jeon, Y.-R., Kim, S., et al.: Influence of oxygen vacancies in ALD HfO_{2-x} thin films on non-volatile resistive switching phenomena with a $\text{Ti/HfO}_{2-x}/\text{Pt}$ structure. *Appl. Surf. Sci.* **434**, 822–830 (2018)
47. Shibuya, K., Dittmann, R., Mi, S., et al.: Impact of defect distribution on resistive switching characteristics of Sr_2TiO_4 thin films. *Adv. Mater.* **22**, 411–414 (2010)
48. Skaja, K., Andrä, M., Rana, V., et al.: Reduction of the forming voltage through tailored oxygen non-stoichiometry in tantalum oxide ReRAM devices. *Sci. Rep.* **8**, 10861 (2018)
49. Zahari, F., Schlichting, F., Strobel, J., et al.: Correlation between sputter deposition parameters and I-V characteristics in double-barrier memristive devices. *J. Vac. Sci. Technol. B* **37**, 061203 (2019)
50. Asanuma, S., Akoh, H., Yamada, H., et al.: Relationship between resistive switching characteristics and band diagrams of $\text{Ti/Pr}_{1-x}\text{Ca}_x\text{MnO}_3$ junctions. *Phys. Rev. B* **80**, 235113 (2009)
51. Hardtdegen, A., Torre, C.L., Cüppers, F., et al.: Improved switching stability and the effect of an internal series resistor in HfO_2/TiOx bilayer ReRAM cells. *IEEE Trans. Electron Devices* **65**, 3229–3236 (2018)
52. Yu, S., Wu, Y., Jeyasingh, R., et al.: An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation. *IEEE Trans. Electron Devices* **58**, 2729–2737 (2011)
53. Niu, G., Calka, P., Huang, P., et al.: Operando diagnostic detection of interfacial oxygen ‘breathing’ of resistive random access memory by bulk-sensitive hard x-ray photoelectron spectroscopy. *Mater. Res. Lett.* **7**, 117–123 (2019)
54. Baeumer, C., Schmitz, C., Ramadan, A.H.H., et al.: Spectromicroscopic insights for rational design of redox-based memristive devices. *Nat. Commun.* **6**, 8610 (2015)
55. Hansen, M., Ziegler, M., Kolberg, L., et al.: A double barrier memristive device. *Sci. Rep.* **5**, 13753 (2015)
56. Woo, J., Moon, K., Song, J., et al.: Improved synaptic behavior under identical pulses using AlOx/HfO_2 bilayer RRAM array for neuromorphic systems. *IEEE Electron Device Lett.* **37**, 994–997 (2016)
57. Stathopoulos, S., Khat, A., Trapatseli, M., et al.: Multibit memory operation of metal-oxide bi-layer memristors. *Sci. Rep.* **7**, 17532 (2017)
58. Sawa, A., Fujii, T., Kawasaki, M., et al.: Hysteretic current–voltage characteristics and resistance switching at a rectifying $\text{Ti/Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$ interface. *Appl. Phys. Lett.* **85**, 4073–4075 (2004)
59. Seong, D.-J., Jo, M., Lee, D., et al.: HPHA effect on reversible resistive switching of Pt/Nb -doped SrTiO_3 schottky junction for nonvolatile memory application. *Electrochem. Solid-State Lett.* **10**, H168 (2007)
60. Yoon, J.H., Song, S.J., Yoo, I.-H., et al.: Highly uniform, electroforming-free, and self-rectifying resistive memory in the $\text{Pt/Ta}_2\text{O}_5/\text{HfO}_{2-x}/\text{TiN}$ structure. *Adv. Funct. Mater.* **24**, 5086–5095 (2014)

61. Mikheev, E., Hoskins, B.D., Strukov, D.B., et al.: Resistive switching and its suppression in Pt/Nb:SrTiO₃ junctions. *Nat. Commun.* **5**, 3990 (2014)
62. Kim, Y., Kwon, Y.J., Kwon, D.E., et al.: Nociceptive memristor. *Adv. Mater.* **30**, 1704320 (2018)
63. Choi, S., Kim, Y., Nguyen, T.V., et al.: Low-power self-rectifying memristive artificial neural network for near internet-of-things sensor computing. *Adv. Electron. Mater.* **7**, 2100050 (2021)
64. Luo, Q., Xu, X., Gong, T., et al.: 8-layers 3D vertical RRAM with excellent scalability towards storage class memory applications. In: 2017 IEEE International Electron Devices Meeting (IEDM), pp. 2.7.1–2.7.4 (2017). <https://doi.org/10.1109/IEDM.2017.8268315>
65. Burr, G.W., Shenoy, R.S., Virwani, K., et al.: Access devices for 3D crosspoint memory. *J. Vac. Sci. Technol. B* **32**, 040802 (2014)
66. Hansen, M., Ziegler, M., Kohlstedt, H.: Double barrier memristive devices for neuromorphic computing. In: 2016 IEEE International Conference on Rebooting Computing (ICRC), pp. 1–8 (2016). <https://doi.org/10.1109/ICRC.2016.7738713>
67. Dirkmann, S., Hansen, M., Ziegler, M., et al.: The role of ion transport phenomena in memristive double barrier devices. *Sci. Rep.* **6**, srep35686 (2016)
68. Hansen, M., Zahari, F., Kohlstedt, H., et al.: Unsupervised Hebbian learning experimentally realized with analogue memristive crossbar arrays. *Sci. Rep.* **8**, 8914 (2018)
69. Strobel, J., Hansen, M., Dirkmann, S., et al.: In depth nano spectroscopic analysis on homogeneously switching double barrier memristive devices. *J. Appl. Phys.* **121**, 245307 (2017)
70. Zidan, M.A., Fahmy, H.A.H., Hussain, M.M., et al.: Memristor-based memory: the sneak paths problem and solutions. *Microelectron. J.* **44**, 176–183 (2013)
71. Kim, H.-D., Crupi, F., Lukosius, M., et al.: Resistive switching characteristics of integrated polycrystalline hafnium oxide based one transistor and one resistor devices fabricated by atomic vapor deposition methods. *J. Vac. Sci. Technol. B* **33**, 052204 (2015)
72. Li, C., Hu, M., Li, Y., et al.: Analogue signal and image processing with large memristor crossbars. *Nat. Electron* **1**, 52–59 (2018)
73. Kiani, F., Yin, J., Wang, Z., et al.: A fully hardware-based memristive multilayer neural network. *Sci. Adv.* **7**, eabj4801 (2021)
74. Sze, S.M.: *Physics of Semiconductor Devices*, pp. 134–196. Wiley (2006). ISBN: 978-0-470-06832-8
75. Tung, R.T.: The physics and chemistry of the schottky barrier height. *Appl. Phys. Rev.* **1**, 011304 (2014)
76. Simmons, J.G.: Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film. *J. Appl. Phys.* **34**, 1793–1803 (1963)
77. Walczyk, D., Walczyk, C., Schroeder, T., et al.: Resistive switching characteristics of CMOS embedded HfO₂-based 1T1R Cells. In: *Microelectronic Engineering. Proceedings of the 17th Biennial International Insulating Films on Semiconductor Conference* **88**, 1133–1135 (2011)
78. Lim, E.W., Ismail, R.: Conduction mechanism of valence change resistive switching memory: a survey. *Electronics* **4**, 586–613 (2015)
79. Yang, J.J., Miao, F., Pickett, M.D., et al.: The mechanism of electroforming of metal oxide memristive switches. *Nanotechnology* **20**, 215201 (2009)
80. Duncan, D., Magyari-Köpe, B., Nishi, Y.: Filament-induced anisotropic oxygen vacancy diffusion and charge trapping effects in hafnium oxide RRAM. *IEEE Electron Device Lett.* **37**, 400–403 (2016)
81. Zidan, M.A., Chen, A., Indiveri, G., et al.: Memristive computing devices and applications. *J. Electroceramics* **39**, 4–20 (2017)
82. Xiong, W., Zhu, L.Q., Ye, C., et al.: Bilayered oxide-based cognitive memristor with brain-inspired learning activities. *Adv. Electron. Mat.* **5**, 1900439 (2019)
83. Bagdzevicius, S., Maas, K., Boudard, M., et al.: Interface-type resistive switching in perovskite materials. *J. Electroceramics* **39**, 157–184 (2017)
84. Chen, H.-Y., Yu, S., Gao, B., et al.: HfO_x based vertical resistive random access memory for cost-effective 3D cross-point architecture without cell selector. In: 2012 International Electron Devices Meeting, pp. 20.7.1–20.7.4 (2012). <https://doi.org/10.1109/IEDM.2012.6479083>

85. Mochida, R., Kouno, K., Hayata, Y., et al.: A 4M synapses integrated analog ReRAM based 66.5 TOPS/W neural-network processor with cell current controlled writing and flexible network architecture. In: 2018 IEEE Symposium on VLSI Technology, pp. 175–176 (2018). <https://doi.org/10.1109/VLSIT.2018.8510676>
86. Valentian, A., Rummens, F., Vianello, E., et al.: Fully integrated spiking neural network with analog neurons and RRAM synapses. In 2019 IEEE International Electron Devices Meeting (IEDM), pp. 14.3.1–14.3.4 (2019). <https://doi.org/10.1109/IEDM19573.2019.8993431>
87. Le, B.Q., Grossi, A., Vianello, E., et al.: Resistive RAM with multiple bits per cell: array-level demonstration of 3 bits per cell. IEEE Trans. Electron Devices **66**, 641–646 (2019)
88. Adam, G.C., Hoskins, B.D., Prezioso, M., et al.: 3-D memristor crossbars for analog and neuromorphic computing applications. IEEE Trans. Electron Devices **64**, 312–318 (2017)
89. Lin, P., Li, C., Wang, Z., et al.: Three-dimensional memristor circuits as complex neural networks. Nat. Electron. **3**, 225–232 (2020)
90. Suri, M., Bichler, O., Querlioz, D., et al.: CBRAM devices as binary synapses for low-power stochastic neuromorphic systems: auditory (Cochlea) and visual (Retina) cognitive processing applications. In: 2012 International Electron Devices Meeting, pp. 10.3.1–10.3.4 (2012). <https://doi.org/10.1109/IEDM.2012.6479017>
91. Zahari, F., Pérez, E., Mahadevaiah, M.K., et al.: Analogue pattern recognition with stochastic switching binary CMOS-integrated memristive devices. Sci. Rep. **10**, 14450 (2020)
92. Wang, S.-Y., Huang, C.-W., Lee, D.-Y., et al.: Multilevel resistive switching in Ti/Cu_xO/Pt memory devices. J. Appl. Phys. **108**, 114110 (2010)
93. Wu, Y., Yu, S., Wong, H.-S. P., et al.: AlO_x-based resistive switching device with gradual resistance modulation for neuromorphic device application. In: 2012 4th IEEE International Memory Workshop, pp. 1–4 (2012). <https://doi.org/10.1109/IMW.2012.6213663>
94. Milo, V., Zambelli, C., Olivo, P., et al.: Multilevel HfO₂-based RRAM devices for low-power neuromorphic networks. APL Mater. **7**, 081120 (2019)
95. Perez, E., Mahadevaiah, M.K., Perez-Bosch Quesada, E., et al.: In-depth characterization of switching dynamics in amorphous hfo2 memristive arrays for the implementation of synaptic updating rules. Jpn. J. Appl. Phys. (2022). <https://doi.org/10.35848/1347-4065/ac6a3b>
96. Alibart, F., Gao, L., Hoskins, B.D., et al.: High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm. Nanotechnology **23**, 075201 (2012)
97. Pérez, E., Pérez-Ávila, A.J., Romero-Zalaz, R., et al.: Optimization of multi-level operation in RRAM arrays for in-memory computing. Electronics **10**, 1084 (2021)
98. Bousoulas, P., Michelakaki, I., Skotadis, E., et al.: Low-power forming free TiO_{2-x}/HfO_{2-y}/TiO_{2-x}-trilayer RRAM devices exhibiting synaptic property characteristics. IEEE Trans. Electron Devices **64**, 3151–3158 (2017)
99. Milano, G., Raffone, F., Luebben, M., et al.: Water-mediated ionic migration in memristive nanowires with a tunable resistive switching mechanism. ACS Appl. Mater. Interfaces **12**, 48773–48780 (2020)
100. Cüppers, F., Menzel, S., Bengel, C., et al.: Exploiting the switching dynamics of HfO₂-based ReRAM devices for reliable analog memristive behavior. APL Mater. **7**, 091105 (2019)
101. Tan, Z.J., Somjit, V., Toparli, C., et al.: Electronegative metal dopants improve switching consistency in Al₂O₃ resistive switching devices (2021). [arXiv:2104.13301](https://arxiv.org/abs/2104.13301)
102. Wang, Z., Yin, M., Zhang, T., et al.: Engineering incremental resistive switching in TaO_x based memristors for brain-inspired computing. Nanoscale **8**, 14015–14022 (2016)
103. Kelly, P.D., Arnell, R.D.: Magnetron Sputtering : A Review of Recent Developments and Applications (2000)
104. Bräuer, G., Szyszka, B., Vergöhl, M., et al.: Magnetron sputtering – milestones of 30 years. In: Vacuum. Selected Papers from the Proceedings of The Tenth International Symposium on Sputtering and Plasma Processes (ISSP 2009), 8th–10th July 2009, Kanazawa, Japan **84**, 1354–1359 (2010)
105. Minami, T., Miyata, T., Yamamoto, T., et al.: Origin of electrical property distribution on the surface of ZnO: Al films prepared by magnetron sputtering. J. Vac. Sci. Technol. A **18**, 1584–1589 (2000)

106. Kersten, H., Deutsch, H., Steffen, H., et al.: The energy balance at substrate surfaces during plasma processing. *Vacuum* **63**, 385–431 (2001)
107. Bornholdt, S., Itagaki, N., Kuwahara, K., et al.: Characterization of the energy flux toward the substrate during magnetron sputter deposition of ZnO thin films. *Plasma Sources Sci. Technol.* **22**, 025019 (2013)
108. Haase, F., Lundin, D., Bornholdt, S., et al.: On the impact of electron temperature in magnetron sputtering benchmarked with energy flux measurements. *Contrib. Plasma Phys.* **55**, 701–713 (2018)
109. Gauter, S., Haase, F., Kersten, H.: Experimentally unraveling the energy flux originating from a DC magnetron sputtering source. *Thin Solid Films* **669**, 8–18 (2019)
110. Ellmer, K., Welzel, T.: Reactive magnetron sputtering of transparent conductive oxide thin films: role of energetic particle (Ion) bombardment. *J. Mater. Res.* **27**, 765–779 (2012)
111. Welzel, T., Ellmer, K.: The influence of the target age on laterally resolved ion distributions in reactive planar magnetron sputtering. *Surface and coatings technology. PSE 2010 Special Issue* **205**, S294–S298 (2011)
112. Thornton, J.A.: Substrate heating in cylindrical magnetron sputtering sources. *Thin Solid Films* **54**, 23–31 (1978)
113. Mott-Smith, H.M., Langmuir, I.: The theory of collectors in gaseous discharges. *Phys. Rev.* **28**, 727–763 (1926)
114. Cherrington, B.E.: The use of electrostatic probes for plasma diagnostics—a review. *Plasma Chem. Plasma Process* **2**, 113–140 (1982)
115. Kersten, H., Kroesen, G.M.W., Hippler, R.: On the energy influx to the substrate during sputter deposition of thin aluminium films. *Thin Solid Films* **332**, 282–289 (1998)
116. Piejak, R., Godyak, V., Alexandrovich, B., et al.: Surface temperature and thermal balance of probes immersed in high density plasma. *Plasma Sources Sci. Technol.* **7**, 590–598 (1998)
117. Piel, A.: *Plasma Physics: An Introduction to Laboratory, Space, and Fusion Plasmas* isbn: 978-3-642-43631-4. Springer, Berlin Heidelberg (2010)
118. Heil, B.G., Czarnetzki, U., Brinkmann, R.P., et al.: On the possibility of making a geometrically symmetric RF-CCP discharge electrically asymmetric. *J. Phys. D: Appl. Phys.* **41**, 165202 (2008)
119. Bienholz, S., Bibinov, N., Awakowicz, P.: Multiple frequency capacitively coupled plasmas as a new technology for sputter processes. *J. Phys. D: Appl. Phys.* **46**, 084010 (2013)
120. Lee, J., Shin, J., Lee, D., et al.: Diode-less nano-scale ZrO_x/HfO_x RRAM device with excellent switching uniformity and reliability for high-density cross-point memory applications. In: *2010 International Electron Devices Meeting*, pp. 19–5 (2010)
121. Huang, H.-M., Wang, Z., Wang, T., et al.: Artificial neural networks based on memristive devices: from device to system. *Adv. Intell. Syst.* **2**, 2000149 (2020)

Open Access This chapter is licensed under the terms of the Creative Commons Attribution 4.0 International License (<http://creativecommons.org/licenses/by/4.0/>), which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license and indicate if changes were made.

The images or other third party material in this chapter are included in the chapter's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the chapter's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder.

