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Self-Aligning Metallic Vertical Interconnect Access Formation through Microlensing Gas Phase Electrodeposition controlling Airgap and Morphology

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This publication reports self-aligning metallic via microlensing gas phase electrodeposition formation. Key operational parameters to fabricate vertical ruthenium and rhodium interconnects (via) with a diameter of 100 nm are discussed. Moreover, airgaps are implemented during the deposition process, which utilizes spark discharge to generate a flux of charged nanoparticles. An inert gas flow transports the nanoparticles through a reactor chamber close to the target substrate. The substrate uses a pre-patterned resist with openings to a silicon/silicon dioxide/metal stack to direct the deposition of the nanoparticles to form localized self-aligning vertical interconnects. Five process parameters were identified, which impact the morphology and conductance of the resulting interconnects: spark discharge power, gas flow rate, microlens via dimensions, substrate surface potential, and in situ flash lamp power. This parameter set enables a controlled adjustment of the via interconnect morphology and its minimum feature size. Gas flow rate in combination with spark discharge power contribute significantly to the morphology of the interconnect. Spark power and microlens via dimensions have the largest influence on the surface potential of the insulating resist cover, which enables a localized microlensing gas phase electrodeposition of a via with a controlled ratio between conducting diameter and airgap.

1. Introduction

The fabrication of integrated circuits remains an exciting field of development. For a long time, Moore's Law was considered the driver of advancing miniaturization. However, with the beginning of this decade and the implementation of the 7 nm technology node, Moor's straight linear line kinks.[1] The dominant technology in recent years has been the implementation of the FinFET with 3-side gate channel control.[2] Although the node size is approaching a limit, new trends are found within the technology node to better utilize the active chip area respectively the active chip volume for semiconductor devices. Trendsetting here are the technologies of gate-all-around field effect transistors (GAAFETs),[3–5] which use stacked nanowires as active channel, and the implementation of multi-bridge-channel field effect transistors (MBCFETs),[4,6–8] which shall use 2D nanoflakes as active channel. However, a pure increase of active devices on a defined chip area respectively in a defined chip volume bring new challenges. The interplay between the Front End of Line (FEOL) processes and the metallization levels (Backend of Line - BEOL) moves more into focus by the extended research and development field so called as Middle of Line. This intermediate section in the chip is interesting, because the distance between the vertical interconnects (via) decreases due to the decreasing dimensions. As a result, the surface to volume ratio of the structures is increasing. This miniaturization has a bad effect on the time constant τ of the system because the ohmic resistance R and the parasite capacity C increase. Taking a closer look to the parameters of R and C reveals that the conductivity σ, the dielectric behavior of the surrounding insulator ε, the vertical length of the interconnect, as well as the distance between the interconnects determine the time constant, which is given by

$$\tau = \frac{1}{f} = R \cdot C = \frac{1}{\sigma} \cdot \frac{\varepsilon \cdot l}{d} \tag{1}$$

With the increasing miniaturization, the smaller via must transport the same current density respectively heat flux and require a long-term stability. In addition, there is another trend from Stanford to revise the computing architecture. In most computer systems, the calculation maximum is limited

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by the Von Neumann bottleneck.[9] This results from the separation of processor and main memory, as well as the bus system in between. The new concept[10] plans an alternating three-dimensional stacking of processors and memory layers. The interconnection between the layers requires mechanically stable, electrically conductive and thermally conductive interconnects. The efficiency of the resulting electrical interconnect depends on the two material constants electrical conductivity and permittivity.

The electrical conductivity shows a strong material dependence in the sub-100 nm range. Below this dimension, the material properties are reversed due to dominating surface effects. Platinum metals—e.g., ruthenium, rhodium, and rhenium—exhibit particularly good conductivities compared to other metals.[11,12] Standard technology node approaches follow a process route, which dry etches more than 99% of a deposited metallic film to achieve the resulting patterns. However, these metals are rare, which means that their use requires a material-saving application and manufacturing process.

In this work the principle of gas phase electrodeposition is adapted, which demonstrated metallic horizontal interconnects in the past and presents itself as very material efficient.[13–15] While the use of direct print methods for packaging metal tracks on flexible substrates has increased in recent years, the number of applications in the sub-micrometer range is rare. Another important material constant for interconnects is the relative permittivity. To keep the interfering capacitances as low as possible, this value should be as close as possible to the minimum of 1 for air. The solution to this problem is the integration of airgaps, so-called air-filled cavities between the conductive tracks.[16] The direct implementation of airgaps is challenging. Localized growth by gas-phase electrodeposition could offer the possibility to selectively decrease the diameter of the via interconnect with the implementation of a surrounding airgap. In this process, metallic nanoparticles are generated in a spark discharge, transported to the substrate by a gas flow, and can subsequently be deposited into layers[17] or localized structures.[13–15,18–20]

While the benefits of material conservation, size reduction through lensing, and surrounding airgaps are beneficial, the process of gas phase electrodeposition has so far been limited by less electrical conductance. The formation of desired 3D shapes that grew out of the charge dissipating openings under the influence of the dynamic evolving lensing funnel like electric field, consist of small metallic nanoparticles. In initial state this high-ohmic nano-interconnect worked perfect as a gas sensor.[15] The aspect of self-growing and self-aligning interconnects becomes particularly interesting when considering the concept of nanoscale interlayer vias (ILV). These become necessary if connections between individual thin chips are to be made possible in the next chip generation, so that computing power can be massively processed in parallel.[10]

This study reports self-aligning metallic via formation through microlensing gas phase electrodeposition controlling airgap and Morphology. Specifically, nanoparticles of the desired metals are produced in a spark discharge. The produced nanoparticles are then transported by an inert gas flow. In combination with a pre-patterned substrate, the particles are guided in the area of use to from self-aligning via interconnects. Moreover, five key process parameters were identified, which impact the shape of the resulting nanostructure, in particular spark discharge power, gas flow rate, substrate surface potential, in situ flash lamp power, and via aspect ratio. This five-dimensional parameter field enables a controlled adjustment of the via interconnect morphology and its minimum feature size.

2. Materials and Methods

Figure 1 provides a schematic overview of the utilized custom-made reactor next to a closer view of the localized via interconnect gas phase electrodeposition working principle. Five adjustable key parameters are the spark discharge power, the transport gas flow rate, the flash lamp power, the microlens size which in turn is adjusted by the patterned insulator on the substrate and substrate bias. Spark power and transport gas flow rate work in a strong interplay which affects mass deposition rate and morphology[17] of microfilms with tailored morphology. Different from flat films, the influence on the formation of tailored vias is reported in this study. Moreover, the electrical conductivity is relevant and rapid thermal annealing using a flash lamp is incorporated, specifically in situ treatment of the localized growing nanostructures to enhance the electrical conductivity and mechanical stiffness of the resulting vertical interconnects.

The spark discharge power is coupled in by two consumable electrode tips with a gap of 1 mm and a plasma voltage of +V = 1000 V. The discharge works under atmospheric pressure conditions and is space limited, which means that the voltage is defined by Paschen´s law. An increase in power results linear in an increase of the plasma current. It causes liberation of electrons from the cathode by positive ion bombardment. This effect depends on the energy of impact and the work function of the cathode material. This type of mechanism is dependent on the gas because both the work function and the formation of positive ions are functions of the chemical nature of the gas.[21] The resulting plasma erodes the electrode material and leads to the production of nanoparticles (generation zone). The production of nanoparticles is dependent on the cathode material including the physical parameter density which correlates with the melting point of the desired material. An adjustable inert/reductive gas flow (5% H2 in N2, inlet diameter 6 mm) transports the nanoparticles for 2 cm to the nearfield of the substrate (transport zone). The motion of particles is gas flow dependent. Figure S1 (Supporting Information) illustrates how the color and shape of the plasma jet changes for various power and gas flow rate. The substrate is fixed on a biased substrate holder (–V = –1000...0 V Bias, diameter 1 cm). An amperemeter measures the deposition current flowing off the substrate. The substrate holder is placed in the focal point of a circular surrounding flash annealing lamp (diameter 6 cm) with a maximum pulse energy of 230 Joules and adjustable frequency. The aim of this flash lamp is an in situ sintering to let individual particles form spherical agglomerates. The result is a compressed dense deposit. The outer walls of the reactor chamber are custom-made out of PMMA. The chamber's diameter is 10 cm, the chamber's height is

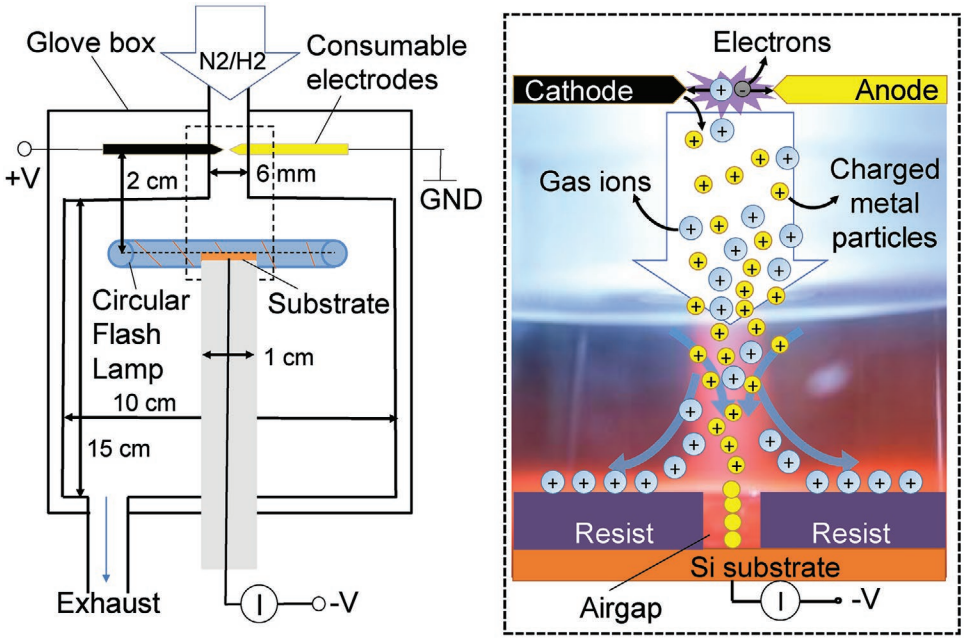

Figure 1. Schematic and dimensions of reactor design next to microlens gas phase electrodeposition method, not drawn to scale. For the background a photograph of the plasma jet is used.

15 cm. The whole chamber is placed in a glove box-controlled nitrogen atmosphere (0.1 ppm O_2 and 1 ppm H_2O level). The schematic (Figure 1, right) details the localized gas phase electrodeposition process, specifically, the interplay between gas ions, charged metal particles and a patterned substrate. The resulting deposition current consists of both species gas ions and charged nanoparticles.[17] The patterned resist forms an electrodynamic lens array. High-mobility nitrogen ions arrive first, charge the resist positive and create a pillow on which subsequent positively charged carriers (nitrogen ions and charged nanoparticles, ratio 50...100:1[17]), are deflected until they reach the charge dissipating biased substrate through the openings in the resist. Under steady state, a flux of positive charges is established through the openings in the resist which provide the access to the charge dissipating substrate. As a result, the nanoparticles start to from localized structures in the openings (deposition zone). The morphology of the resulting structure including electrical and mechanical properties are dependent on three parameters: i) spark discharge power, ii) transport gas flow rate, iii) flash lamp power.

i) Spark discharge: In the Paschen regime, the spark discharge is current driven and an increase of the current between the consumable electrodes increases the number of charged species including nanoparticles in the spark region and the entire reactor. ii) The gas flow (a crossflow) exerts a force on the charge species and is used, up to a certain point, to move charged carriers from the plasma region to the substrate. The flux of charged species and volume number concentration increase and reach a maximum before they drop at excessive gas flow rates. The gas flow is highly relevant for directed transport toward the substrate and impact the dissipation current which is recorded at the substrate. The gas flow distribution can be seen as an equivalent electrical potential distribution. iii) The substrate bias impacts the collection process: a negative bias increases and a positive bias reduces the directed transport to the substrate, respectively. A sufficiently large positive bias voltage can be used to offset the flow directed transport and zero the deposition current. At low gas flow rate the transport is mainly driven by the electric field, while high gas flow rates lead to a gas flow rate driven transport condition. This variable condition affects the morphology and the deposition rate of deposited films. Low spark discharge power and low gas flow rates lead to fast growing dendrites, while high spark power and high gas flow rate lead to closed and densely packed films. A stronger bias potential increases the deposition rate.[17]

Two important parameters have not been studied for gas phase electrodeposition: iv) aspect ratio of the insulator patterns on the substrate as well as v) floating insulator potential. These parameters are examined in this study.

3. Results and Discussion

Figure 2 discusses the (a) morphology as a function of gas flow rate and plasma power next to a computational study of the (b) evolving potential funnel to explain the increased focus at high plasma powers and the increase in the (c) deposition current reaching a maximum at 8000 sccm and 10 W. The nanostructures are deposited for 1 min in 1 µm AZ 1505 resist openings on 1 cm^2 silicon test chips with repeating openings in both directions with a pitch of 10 µm. The spark discharge power was coupled in by two parallel gamma high voltage power sources. The substrate bias potential is constant for all presented deposits at −500 V. Going from left to right at a spark discharge power of 2.5 W the influence of the gas flow rate gets visible. A low gas flow rate leads to dendrites, while higher gas flow rates pack deposits more densely. This influence has been described before by a reduced primary particle size leaving the

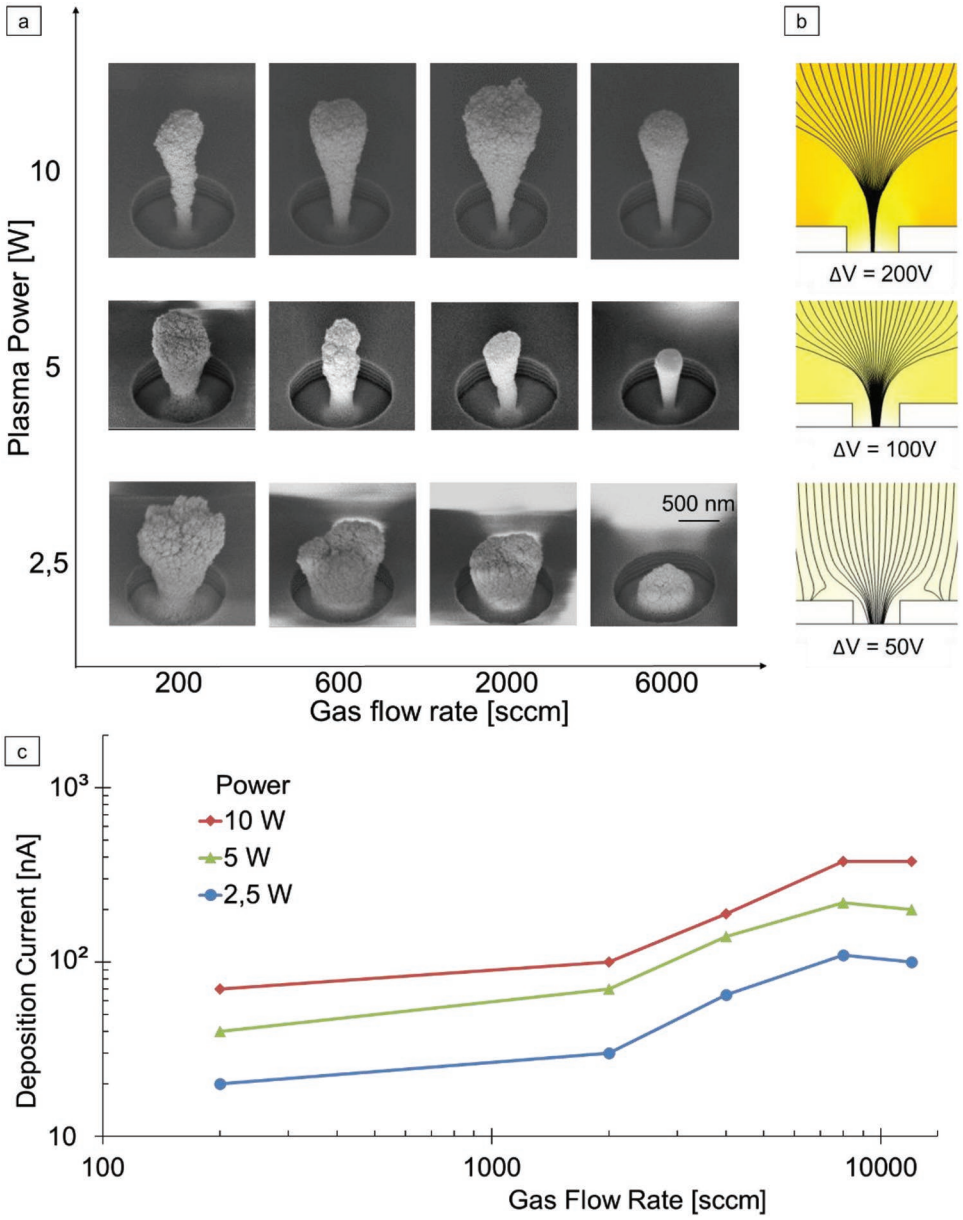

Figure 2. a) Two-parametric analysis of localized deposits at different spark discharge powers and at different gas flow rates next to b) a computational study of the evolving potential funnel at different plasma powers and c) the spark discharge power and gas flow rate dependent deposition current.

spark discharge generation zone at higher gas flow rates.[13,22] The interesting part of Figure 2a is the addition of the parameter spark discharge power. Going from bottom to top the figure reveals that at any gas flow rate the increasing spark discharge power reduces the diameter of the resulting nanostructure. A spark discharge power of 2.5 W leads to a resulting diameter of 600 nm in a 1 µm resist opening, while a spark power of 10 W reduces the diameter to 200 nm. A second point can be drawn as observed at microfilms. The combination of spark discharge power and gas flow rate is the driver to control the morphology of localized deposited nanostructures using gas phase electrodeposition. Low spark power and low gas flow rates lead to broad growing dendrites, high spark power and high gas flow rate lead to localized and dense structures. The results of these depositions are very well reproducible. During the tests, ≈100 samples of 1 cm^2 size were produced at different powers and gas flows. The yield is well above 99% and around 65% of the produced material get collected into the resist openings. No material is deposited onto the resist, a rest of 35% of the produced material gets spilled into the exhaust by the gas flow velocity. A scaling to 4 inch or larger has not yet been carried out. For these experiments the reactor would require some modifications including more plasma sources and a smart shower head inlet design.

Figure 2b shows a computational study of the evolving potential funnel at the three different plasma powers. The boundary conditions for the used electrical currents model were taken from a previous publication of our own.[17] With increasing

plasma power, the resist becomes more charged. While for 2.5 W a potential of 50 V is reached, the surface potential for 10 W rises up to 200 V. However, the exact driver for this process has not been studied yet. The computation explains the observed behavior in Figure 2a; increases in the plasma power lead to a tighter focus, and the observed increase in focus can be explained using the buildup of a higher surface potential, a floating potential on the insulating resist surface, i.e., the double layer potential between the insulating resist surface and conducting substrate increases and leads to a higher fringing field.

Figure 2c represents corresponding current curves at different spark discharge power and gas flow rate. Qualitatively, all follow the same trend. Looking at the curve for 2.5 W, it can first be observed that it increases from low gas flow rate to higher gas flow rate. It is noticeable that the steepest step occurs between 2000 sccm and 8000 sccm. Above 8000 sccm, the current saturates. This qualitative trend is the same for all three curves (2.5 W to 10 W). Comparing two or all three curves, the substrate current increases with increasing plasma power. A doubling of the plasma power leads to a doubling of the measured substrate current. There are two possible reasons or a combination of both for this effect. Either the charge carriers are transported more effectively to the substrate, or the number of charge carriers has increased. The generation of the charged particles in the discharge region is a current driven space-limited spark discharge. A typical discharge voltage is ≈1000 V mm^{-1} gap distance. We used a 1 mm electrode gap in all experiments. In the operation window, a linear increase of the power results roughly in both, a linear increase of the spark current and a linear increase in the number of charged carriers in the spark region. In other words, the number of gas ions and metal particles is increased in the spark region and ultimately more of these species are transported to the substrate by the crossing gas flow.

Based on the knowledge gained from the depicted microlenses in Figure 2a and the computation data in Figure 2b combined with the current behavior from Figure 2c, the following conclusion can be drawn: twice as much plasma power generates twice as many charge carriers. Thus, the gas flow transports twice as many charge carriers to the substrate surface. These need to flow twice as fast through the openings. While the plasma power influences the charge carrier concentration, the gas flow rate contributes significantly to the morphology. Low gas flow rates lead to dendrites. High gas flow rates lead to denser structures.

The increasing surface potential due to the charging insulating resist opens the question, whether the dimensions of resist openings influence the value of the floating potential (surface potential) and subsequently the level of focus or filament where the charge carriers flow through. **Figure 3** studies the level of focus as a function of the resist thickness. Moreover, the influence of the resist opening on the deposition current at various flow rates is established. Higher flow rates lead to an increase in the deposition current. A picture of filaments and transport that is dominated by the physical dimensions of the openings can be established. Figure 3a provides a starting point for the discussion depicting a cleaned substrate, where a previous patterned resist layer is removed before deposition. The contrast of the openings is still visible in the scanning electron microscope (SEM) micrograph due to the thin HDMS primer residue from the spinning process. Nickel nanoparticles are deposited for 3 min at a spark power of 2.5 W and a gas flow rate of 6000 sccm. The micrograph shows that a few

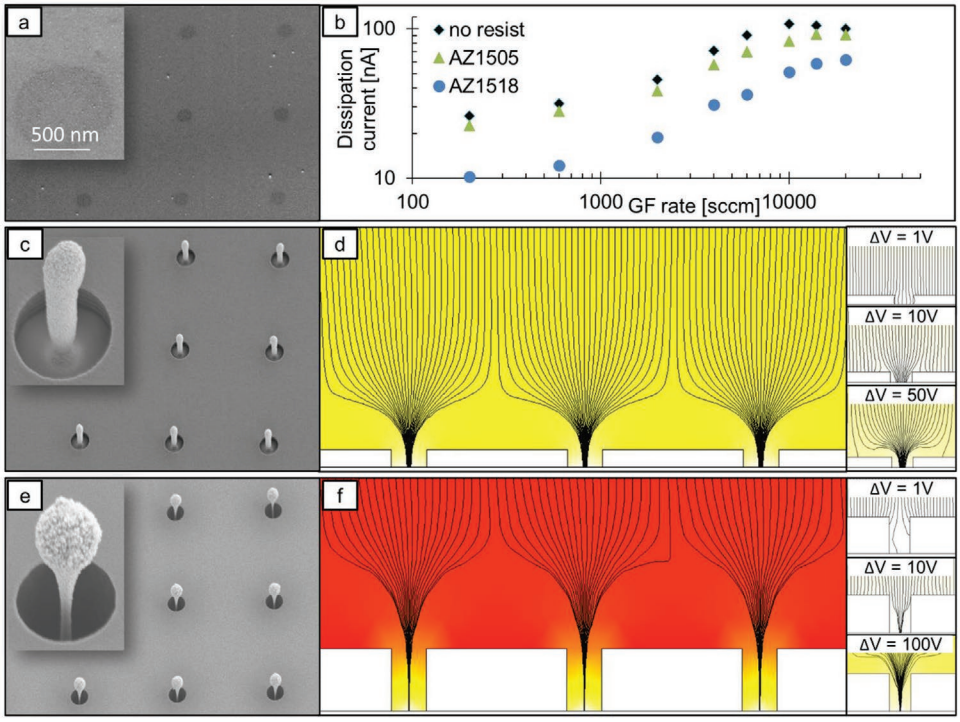

Figure 3. SEM micrographs of resulting structures with a) no resist, c) 500 nm thick resist, and e) 1800 nm thick resist. b) Deposition currents, and d,f) surface potential as a function of photo resist pattern thickness (no resist, 500 nm, and 1800 nm).

single particles deposited randomly on the substrate surface. The data points in (b, black diamond) depict corresponding current values at various gas flow rates. An increase in the gas flow from 200 sscm increases the deposition current. A limit is reached at fairly high flow rates of 10 000 sscm. The depicted curve follows the previously reported behavior where film like deposition on a similar bare nonpatterned substrate without lensing structures was studied.[17] Different from prior results the resist based lensing structures 500 nm thick (center, c and d) and 1 µm thick (bottom, e and f) are added to this discussion. The patterned resist, 1 µm circular resist openings in 500 nm thick AZ1505 (green triangles) and 1800 nm thick AZ1518 (blue spheres) leads to a reduction of the total current that is transported to the substrate. Moreover, a thicker resist yields a higher reduction, the thicker the insulating resist, the lower is the conductance of each opening.

Figure 3c shows the corresponding micrograph for a three-minute-long deposition in AZ1505 resist openings, returning back to a constant flow rate of 6000 sscm, previously used in (a). The ratio between opened area and chip area is 0.7%, which means the opened area is reduced by a factor of more than 100-fold going from image (a) to (c). Going from completely open to 500 nm thick resist the current drops just by a few percent. This means in the first order that nearly all nanoparticles, which are deposited randomly in (a), are collected in the openings of (c). The charged insulating resist funnels the nanoparticles into a diameter of 300 nm, in other words, to 0.1% of the complete chip area. Figure 3d adds a corresponding computation of the electric field distribution. Structures grow in this specific manner, if the surface potential on top of the resist is more than 50 V. Going to a thicker resist of 2 µm AZ1518, the deposition occurs much more focused (e). In other words, the surface potential needs to increase to at least 100 V (f). So far, another conclusion can be drawn that enhances the understanding of gas phase electrodeposition. The funneling effect of an insulating resist opening increases as the aspect ratio of the opening increases. Together with the enhanced control of the morphology (by spark power and gas flow rate) and the surface potential adjustment on top of the insulating resist (by spark power and resist thickness) the localized microlensing gas phase electrodeposition enables a controlled miniaturized deposition method for vertical interconnects (via) which will be further discussed in the next section.

Figure 4 presents self-aligning metallic via formation through microlensing gas phase electrodeposition. The reactor is operated with the same geometries, flash lamp conditions (≈190 W s) and 5% forming gas inlet as in Figures 1–3. The schematic in (a) shows that the stack of the substrate is slightly changed for via formation. The substrate is again patterned. However, it holds additional layers: a semiconducting silicon surface (bottom electrode), a 1 µm thick silicon dioxide insulating spacer, a 100 nm thick chromium layer (top electrode) and a 500 nm thick patterned photoresist to cause lensing and self-aligning via formation, between the top and bottom electrode. The fabrication is detailed in the Experimental Section. Based on knowledge gained from Figures 2 and 3, a deposition algorithm is utilized. Initially, the growth process starts at a power of 10 W and a gas flow rate of 8000 sccm. This

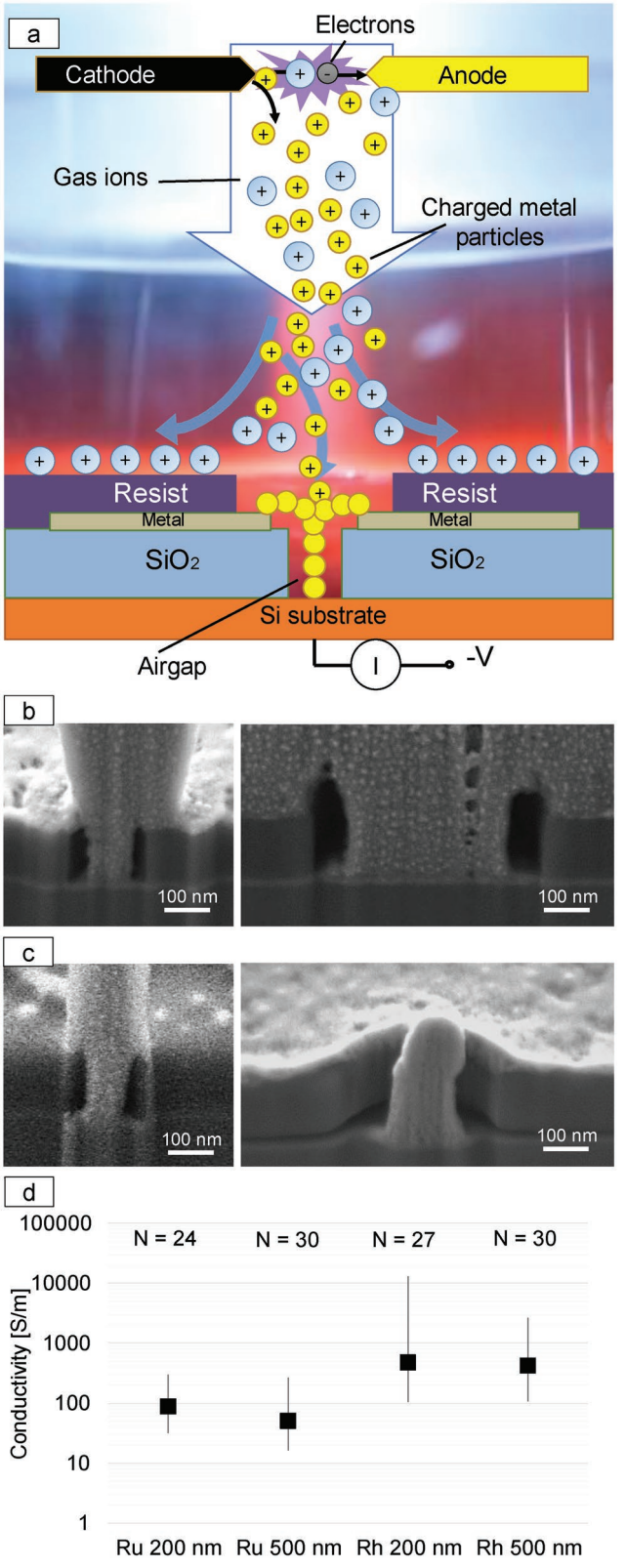

Figure 4. a) Schematic for vertical interconnect formation, b) resulting SEM micrographs for ruthenium deposition and c) rhodium deposition, d) conductivity measurements.

focuses the incoming nanoparticles into the center and the via grows vertically upward from the bottom on the silicon substrate. After 45 s, the plasma power of the particle source is reduced to 2.5 W and the process runs for another 30 s. The reduction of the plasma power is used to reduce the carrier concentration, which in turn reduces the floating potential and decreases the focus. As a result, the material grows more laterally, and an interconnect is formed between the top and bottom electrode.

The SEM micrographs show ruthenium (b) and rhodium (c) interconnects deposited using this approach. For imaging, the samples were prepared using focused ion cuts using a Zeiss FIB Auriga 50 system. The left part shows 200 nm insulator openings. To the right are 500 nm insulator openings. The sub-microstructures are well centered in the openings. Experimentally, we used 10 W plasma power to achieve a sufficient focus and to create a desired airgap between the insulator and the conductor itself. The small interconnects measure 100 nm in diameter and are surrounded by 50 nm air gap between the conductor and the surrounding SiO2. The airgap increases to 80 nm using the larger via size. Unfortunately, rhodium is less stable in the FIB cutting process. It ablates faster than ruthenium. In other words, we lost material during the preparation. The depicted half cut via images are approximate images. Moreover, concerning the FIB samples, we extended the deposition time by additional 20 s to prepare a surface with mushrooming like vias, which were more stable in the FIB cutting process. Concerning the Rhodium via formation required changes to the design of the opening. The lens forming resist opening was increased from 0.4 µm to 2 µm in the small and from 1 to 5 µm in the large via design, respectively. The increased upper layer causes a wider top contact formation.

Figure 4d plots values of the electrical conductivity of the fabricated vias. Between 24 and 30 interconnects were characterized. Figure S2 (Supporting Information) depicts a typical I/V curve crowd. We directly measured the resistance and calculated the conductance using a linear measured approximation for resistor length and width. The first thing to note is that contrary to an expected trend the conductivity of the 200 nm patterns is higher than the conductivity of the 500 nm patterns. In addition, rhodium conducts better than ruthenium. The conductivities of the ruthenium range from 20 to 300 S m^{-1}. Rhodium, on the other hand, reaches 100 to slightly more than 10^4 S m^{-1}. Compared to bulk material, these conductivities are significantly lower and require further optimization of the process. However, when compared with values from printed electronics, which operate in the 10 µm range, they are in the same order of magnitude.[23] First and foremost, this experiment was a first demonstration of the via formation. The process is based on the localized collection of nanoparticles by electrostatic microlens. Further development steps are necessary to meet the requirements of a semiconductor technology application.

4. Conclusion

The combination of spark discharge power and gas flow rate is the driver to control the morphology of localized deposited nanostructures using microlensing gas phase electrodeposition. An increasing gas flow rate narrows the generated primary particle size distribution to a smaller mean value and standard deviation, creating more round particles. Increasing plasma power creates larger more round particles, which carry more heat energy. Increased power increases the number concentration of charged species in the reactor as well. Low spark power and low gas flow rate lead to broad growing dendrites; a combination of low spark power and high gas flow rate creates dense structures at low growth rate with a broad foot. Low gas flow rate in combination with high spark power creates focused structures with a porous morphology. High spark power and high gas flow rates lead to localized and dense structures. The funneling effect of an insulating resist opening increases as the aspect ratio of the opening increases. To achieve the actual via deposition, an exact matching of generation power (45 s 10 W, then 30 s 2.5 W), gas flow rate (8000 sccm) and top resist patterns (ratio bottom via pattern to top resist pattern 1:5) is required. Thus, an interconnect diameter of 100 nm with 50 nm surrounding airgap is achieved for the 200 nm silicon oxide openings. Standard through silicon vertical interconnects use copper and tungsten. The deposition is standard electro plating. This type of deposition always faces great challenges. The via should fill up void free. At the same time, care must be taken to ensure that too rapid growth does not occur only at the edges. Especially with large aspect ratios, the fast growth quickly leads to voids. After oxidation of the opening, a seed layer must be applied to the sidewalls. The goal is an optimum of conformal and super conformal growth. The aspects mentioned show that the TSV standard process is very susceptible and optimized down to the smallest detail.[24–26]

Our process is based on the localized collection of nanoparticles by electrostatic microlenses. The material is focused to the center of the via, which is a clear difference compared to the standard electroplating process. The goal of this study was to get a first handle on the geometry of the deposition/growth process, i.e., to connect two points in a vertical direction with some level of widening toward the top to connect a secondary surface. This initial goal was achieved and a current flow was established. Future research needs to research process parameters to study and adjust the conductivity of these connections. The parameter space is large, and a combinatorial approach and full-scale study should be implemented to get both handles on geometry and conductivity. Further experiments are necessary in which additional applications should be developed. In addition to upscaling, through-hole gas phase electrodeposition as a pure TSV would also be conceivable. Another possibility would be to grow stacked chips together. The advantage would be that many small interconnects could distribute the power and heat transport in the overall system in a decentralized, massively parallel manner, so that the component lifetime might become less susceptible to electromigration. On the other hand, however, it must be investigated how long sub 1 µm interconnects survive the endurance test mechanically and electro technically. While there is research to be done, it would be beneficial. The process would be self-aligning, localized, additive, material efficient, open to all metals, potentially some semiconductors, and materials that are difficult to process at low temperatures.

5. Experimental Section

Reactor Design: Customized PMMA (Evonik) chamber, 6 mm inlet tube, 1 mm metallic electrodes from Advent RM, gap of 1 mm, plasma voltage of +V = 1000 V, inert/reductive gas flow (5% H2 in N2, distance spark-substrate 2 cm, biased substrate holder (–V = –1000...0 V Bias, diameter 1 cm), Fluke 87 RMS Multimeter for deposition current measurement over inner resistor of 10 M Ohm, circular surrounding flash lamp (diameter 6 cm, max. 230 W s), chamber's diameter 10 cm, height 15 cm, surrounded Mbraun glove box with controlled ambient conditions (0.1 ppm O_2 and 1 ppm H_2O level).

Sample Preparation Figures 2 *and* 3: 1 µm resist patterns in AZ1505 and AZ1518 on top of p-type 525 µm thick silicon prepared with HMDS primer and Suess MA8 chrome mask aligner.

Sample Preparation Figure 4: Si 4″ Wafer 525 µm, on top a stack of silicon dioxide 500 nm, chromium 100 nm, LP-CVD silicon dioxide 25 nm, three e-beam lithography steps with ARP 6200.13, Allresist GmbH, 500 nm. First, the 25 nm silicon dioxide was dry etched in a fluoric plasma ICP process (300 W, 0.4 Pa, HF-power 75 W, 440 s duration, system: Sentech SI-500 F, CHF3/SF6 = 4:1). The metallic layer was etched after a second lithography step in a chloric plasma ICP process step (Sentech SI-500 Cl, 900 s, Cl2/O2 = 10:1, 500 W, HF-Power 15 W, 0.5 Pa). Finally, in a third lithography step, the top resist was patterned. FIB cuts in Zeiss Auriga 50.

Electric Field Computation: Done in Comsol with electrical currents model, top of resist was floating parameter, boundary conditions for potential drop were taken from literature[17] (previous own publication).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

airgaps, interconnects, ruthenium, rhodium, via

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