Design Methodology and Implementation of Fully Passive RFID SoC with Temperature Sensor

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Abstract

This dissertation presents the methodology and implementation of a fully passive RFID SoC with temperature sensor to reduce supply noise for high accurate wireless temperature measurement. The analysis of the state-of-the-art standalone temperature sensors and the RFID wireless temperature sensors reveals a design challenge that the RFID sensors suffer significantly from the supply noise, due to the RFID communication. In order to improve sensor accuracy without making too many compromises, this dissertation presents the following scientific contributions. First, a time-domain low-voltage low-power temperature sensor is proposed to achieve high accuracy without using a highly complex $\Sigma\Delta$ ADC with low sampling rate . In addition, the methodology for the analysis of supply noise is developed for the generation, the amplification and the digitization of the supply noise. The analysis results show that the supply noise is distributed over a wide frequency spectrum, while the noise in the communication frequency band is amplified by the power management unit. For the analysis of noise digitization by the sensors, this proposed temperature sensor achieves the best-in-class DC supply sensitivity while it still suffers from AC ripple. Therefore, the supply noise generated by RFID communication will significantly affect the sensor performance. The final optimization at system level is achieved by introducing a serial readout command that significantly reduces the supply noise for the sensor readout. The experimental results show that this proposed RFID temperature sensor achieves $\pm 0.4\,^{\circ}\mathrm{C}$ (3σ) from $0\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$,

which is the highest accuracy with the largest operational range compared to the currently reported state-of-the-art RFID temperature sensors. The new RFID command improves the resolution of this RFID temperature sensor by a factor of 16.

Kurzdarstellung

Diese Dissertation stellt die Methodik und die Implementierung eines vollständig passiven RFID SoC mit Temperatursensor zur Reduzierung von Versorgungsrauschen für eine hochgenaue drahtlose Temperaturmessung vor. Die Analyse der modernen eigenständigen Temperatursensoren und der drahtlosen RFID Temperatursensoren zeigt eine Design Herausforderung, dass die RFID Sensoren aufgrund der RFID Kommunikation erheblich unter dem Versorgungsrauschen leiden. Um die Sensorgenauigkeit zu verbessern, ohne zu viele Kompromisse einzugehen, stellt diese Dissertation die folgenden wissenschaftlichen Beiträge vor. Zuerst wird ein Zeitdomain Niederspannungs Niederleistungs Temperatursensor vorgeschlagen, um eine hohe Genauigkeit zu erreichen, ohne einen hochkomplexen ΣΔ ADC mit niedriger Abtastrate zu verwenden. Darüber hinaus wird die Methodik zur Analyse von Versorgungsrauschen für die Erzeugung, Verstärkung und Digitalisierung des Versorgungsrauschens entwickelt. Die Analyseergebnisse zeigen, dass das Versorgungsrauschen über ein breites Frequenzspektrum verteilt ist, während das Rauschen im Kommunikationsfrequenzband durch das Power Management Unit verstärkt wird. Für die Analyse der Rauschdigitalisierung erreicht dieser vorgeschlagene Temperatursensor die beste DC Versorgungsempfindlichkeit seiner Klasse, während er noch unter Wechselstromwelligkeit leidet. Daher wird das durch die RFID Kommunikation erzeugte Versorgungsrauschen die Sensorleistung erheblich beeinflussen. Die abschließende Optimierung auf Systemebene wird durch die Einführung

eines seriellen Auslesekommandos erreicht, das das Versorgungsrauschen für die Sensorauslesung deutlich reduziert. Die experimentellen Ergebnisse zeigen, dass dieser vorgeschlagene RFID Temperatursensor die Genauigkeit von ±0.4 °C (3σ) von 0 °C bis 125 °C erreicht. Die ist höchste Genauigkeit mit der größten Arbeitsbereich im Vergleich zu den derzeit berichteten modernen RFID Temperatursensoren. Der neue RFID Befehl verbessert die Auflösung dieses RFID Temperatursensors um den Faktor 16.

Preface

My motivation to solve analog design problems always drives me to analyze the crucial factor of the problem, to develop a better topology and to push the performance to its limits. The present work is a compilation of the results and insights collected during my time at IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH), Ilmenau, Germany. With a working atmosphere of open, support and fun, the ideas of this dissertation have been slowly but fully developed, implemented and tested.

My research was part of three projects. The *GreenSense* [62] project has been funded by the "Land" of Thüringen (Ministry of Economics, Labour and Technology) and the European Social Fund (ESF) under the reference 2011 FGR 0121. The *ADMONT* [61] project has received funding from the ECSEL Joint Undertaking under grant agreement No 661796. This Joint Undertaking has received support as Innovation Action from the European Union's Horizon 2020 research and innovation programme, the German Federal Ministry of Education and Research (BMBF) and Finland, Sweden, Italy, Austria, Hungary. The IMMS sub-project "Design of intelligent in vitro diagnostic und bioanalytical sensor and actuator system" has received funding under the reference 16ESE0057. The *RoMulus* [63] project is supported within the Research Programme ICT 2020 by the German Federal Ministry of Education and Research (BMBF) under the reference 16ES0362.

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Jun Tan
Erfurt, 26th September 2019

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Chapter 1

Introduction

1.1 Radio Frequency Identification (RFID)

Remote identification and control of the objects without physical contact was first introduced during World War II [39]. After thirty years, this advanced military technology is started to be used in civilian applications [22]. In the 21st century, this Radio-frequency identification (RFID) technology [1] exploded and became part of everyday life. Today, RFID is evolving in even more areas, bringing wireless connectivity to millions and millions objects.

The typical RFID system consists of an interrogator (reader), a transponder (tag) and a server (data processing). The RFID tag is a tiny integrated circuit with an antenna. The RFID reader queries tags for information stored on them. This information can be their static identification numbers or user defined data. The server processes the data obtained from the readers.

The traditional applications of RFID are access control and asset tracking in manufacturing, retail and logistics businesses. Recently, these application scenarios have been extended to the area that has never been so large before. In [70] (Fig. 1.1 (a)), MIT researchers are developing a system that enables

drones to read RFID tags from a relatively long distance while identifying and locating the objects. The technology can be used in large warehouses to continuously monitor and locate individual items to prevent inventory mismatches. In [68] (Fig. 1.1 (b)), cattle tracking using RFID has been approved by the U.S. Department of Agriculture (USDA) in conjunction with the agency's Animal Identification Number (AIN) system. In [75] (Fig. 1.1 (c)), the payment RFID wristband enables contactless and cashless payment that is simple, fast and secure.

Fig. 1.1 The application scenario of RFID is widely expanded.

Passive RFID sensor tags have attracted increasing attention in the last decade. With energy harvesting, RFID communication and sensor functionality, passive RFID sensor tags are suitable for a wide range of applications involving Wireless Sensor Networks (WSN) and the Internet of Things (IoT) [35, 59].

In [71, 56] (Fig. 1.1 (d)), food safety can be tested by changing from the wireless signals emitted by RFID tags when the signals interact with food. The technology can prevent food contamination without modifying the current

RFID tag hardware. In [57] (Fig. 1.1 (e)), the UV light can be detected by a tiny RFID sensor that can be affixed to the thumbnail. The sensor readout is accomplished by the NFC enabled smart phones. In [79] (Fig. 1.1 (f)), the moisture condition can be measured with a UHF RFID tag in harsh industrial environments such as construction, energy, healthcare, automotive production and military.

1.2 High-density multi-mode RFID smart sensor network

The vision of the application scenario [62] of this dissertation is based on discussions with local companies and research institutes to develop an innovative sensor solution for the market expansion of bioanalytics and medical diagnostics. In the bioanalytics and medical engineering, there is a growing need for sensors that require rapid fluid analysis and long-term monitoring of patient vital function.

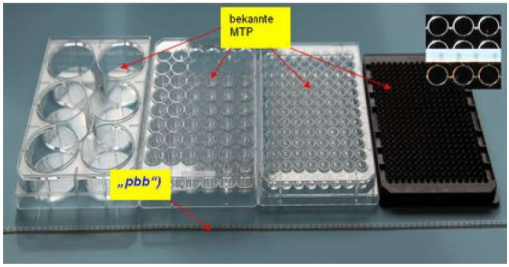


Fig. 1.2 Microtiter plates for the bioanalytics [65]

Fig. 1.2 shows an example of microtiter plates (MTP) in bioanalytics for parallel analysis of a large number of individual samples (e.g. cell cultures). The goal is simultaneous, contamination-free acquisition of various physical and chemical parameters in extremely dense arrays of liquid samples with RFID

micro-sensors (see Fig. 1.3). This results in the following general requirements for the sensors and the sensor network:

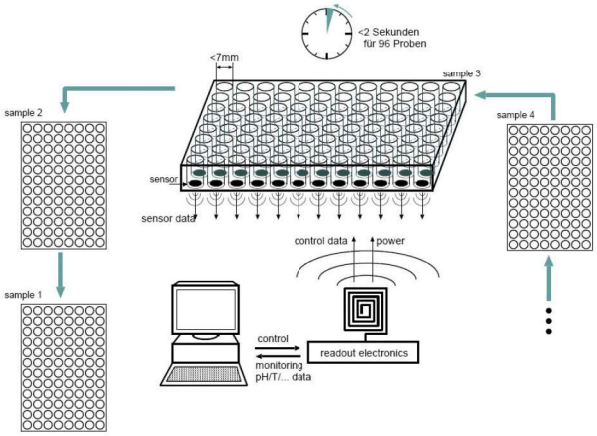


Fig. 1.3 Rapid analysis of liquid samples in microplates [62].

- Extreme miniaturization of the sensor nodes, whose permissible size is limited by the size of the sample container,
- Multi-mode integrated Smart Sensor, such as temperature, pH-value, and turbidity etc,
- Contact-less power supply and data transmission (e.g. via RFID),
- Extremely low power consumption to avoid heat transfer to samples,
- Very fast addressing and reading of a complete array of several hundred samples,
- Low manufacturing cost per sensor unit.

1.3 Technology overview and related state-of-the-art works

This dissertation utilises several technologies to address the challenges. Many of them have been further developed and improved. The technology map is shown in Fig. 1.4. In the following sections, some important technologies are introduced in detail.

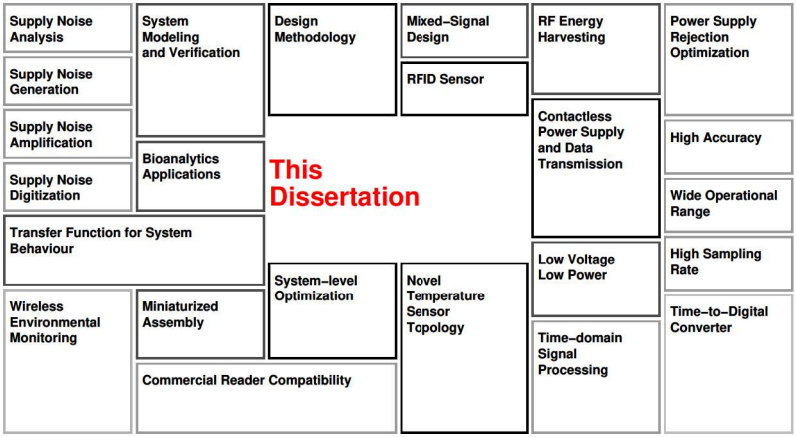


Fig. 1.4 Technology map of this dissertation

Design methodology

The V-diagram [83] is a graphical representation of a system development life cycle and it is widely applied in software development. It is also widely used for design methodology in analog and mixed-signal application specific integrated circuit (ASIC) designs.

On the left, the design is a top-down approach. In this approach, the overview of the system is first formulated and specified, without details. With the design goes to a deeper level, the details are revealed in the sub-systems. On the right,

verification is a bottom-up approach. In contrast to the design phase, verification begins at a lower level in the individual sub-systems. If the system fails verification, the design is reinitialized at the same level for further iteration.

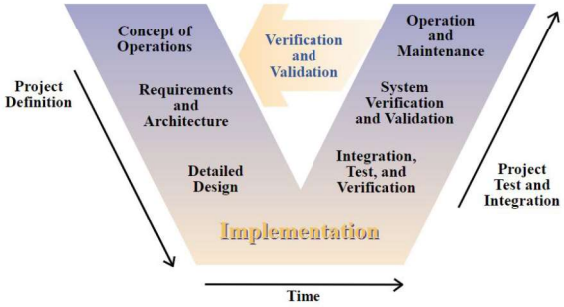


Fig. 1.5 The V diagram [83] is originally used in software development. It is also used in the ASIC designs.

Low-power temperature sensor

CMOS on-chip temperature sensors are being widely adopted for applications that require highly accurate and energy efficient cost-effective solutions for temperature acquisition. These include low-power sensing applications in biomedical, life science, and logistics fields.

According to recent temperature sensor survey [69, 49], CMOS on-chip temperature sensors can be categorized into three major types.

Voltage-domain sensors use a temperature-dependent voltage source and a voltage ADC to convert a temperature signal into a digital code, e.g. [31, 37]. In Fig. 1.6, the sensor core generates two voltages: temperature dependent V_{IN} and temperature independent V_{REF}. The ADC evaluates V_{IN} using the reference voltage V_{REF} and generates the digital code D_{OUT}.

In [31], the topology is improved by a bias circuit, a bipolar core and a $\Sigma\Delta$ ADC (Fig. 1.7). The voltages ΔV_{BE} and V_{BE} are both temperature dependent,

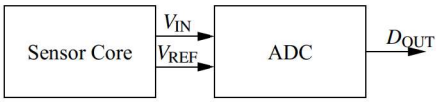


Fig. 1.6 The block diagram of a voltage-domain temperature sensor.

while the reference voltage is built inside the ΣΔ ADC using switched-capacitor circuits. The design utilizes complex ADC topology and design techniques to achieve a high accuracy of ±0.1 °C (3σ) in a wide temperature range (−55 °C to 125 °C). On the other hand, the design consumes 75 µA under 2.5 V supply voltage in a 0.7 µm CMOS technology. Due to the "incremental" natural of the ΣΔ ADC, a single 16-bit digital output can only be generated after several hundred clock cycles, so the conversion time of this design reaches only 100 ms. The supply sensitivity is 0.03 °C/V.

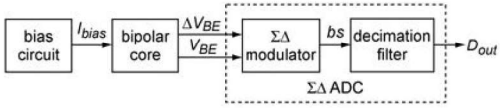


Fig. 1.7 Block diagram of the voltage-domain temperature sensor [31].

In [37], the design is improved by a zoom ADC that combines SAR and ΔΣ principles. A high accuracy up to ±0.15 °C was achieved in a temperature range from −55 °C to 125 °C with a power dissipation of 5.1 µW. Compared to [31], the conversion time is improved to 5.3 ms, while the supply sensitivity is punished to 0.5 °C/V.

Time-domain temperature sensors [32] consists of a temperature-to-pulse generator (delay generator) and a time-to-digital converter (TDC). The delay generator generates a digital pulse with a temperature-dependent delay, e.g. [32, 23, 12, 52]. The time-to-digital converter (TDC), which can be implemented with a simple digital counter, measures the delay and generates a corresponding output code. Fig. 1.8 shows the typical topology of time-domain temperature

sensor. The delay generator is normally implemented by SC circuits [23] or inverters [32, 12, 52].

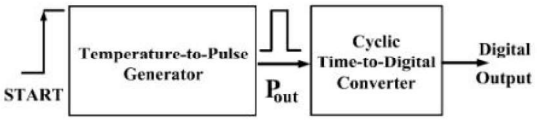


Fig. 1.8 Block diagram of the time-domain temperature sensor [32].

In [12], an inverter-based delay generator in [32] is improved with SAR logic to achieve an inaccuracy of –0.4 °C to 0.6 °C from 0 °C to 90 °C after a two-point calibration. The average power dissipation of the sensor is 36.7 µW with a conversion rate of 2 Samples/s.

[23] introduces an ultra-low-power (ULP) on-chip CMOS temperature sensor with simple structure. In Fig. 1.9, the delay generator is composed of voltage-to-current (V-to-I) converters, SC circuits and inverter-based comparators. The temperature-dependent bias voltages V_{PTAT} and V_{CTAT} are converted into temperature-dependent bias currents in the V-to-I converters. The current discharges the voltages of the SC circuit, after the capacitor is reset to the supply voltage. The inverter-based comparator compares the SC voltage to its own threshold voltage to generate the timing signal. The proposed temperature sensor with 100 nW and 25 Samples/s was reported. It achieves an inaccuracy of –0.8 °C to 1 °C from –10 °C to 30 °C with a sampling rate of 33 Samples/s. The main challenge of this topology is that the inverter-based comparator has a various threshold voltage due to the process-voltage-temperature (PVT) variation. The SC circuit is bound to the supply voltage during the reset phase, so that it is also sensitive to the supply voltage variation. Due to its narrow temperature range, it is restricted to a small range of applications.

The third class of temperature sensors operates in the *frequency domain*, e.g. [16, 18]. They use similar structures as the previous type but deliver

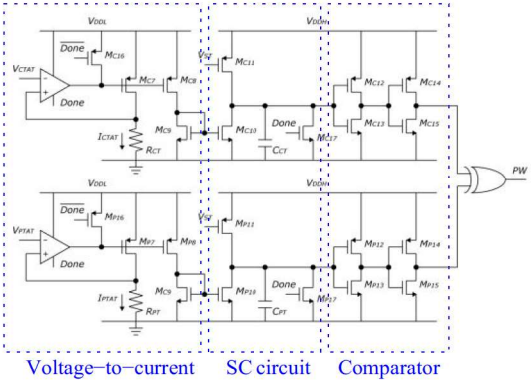


Fig. 1.9 Block diagram of the delay generator in [23].

temperature-dependent frequencies. The sensor reported in [16] achieves −1.6/3 °C inaccuracy in the range from 0 °C to 100 °C and consumes 200 nW.

RFID sensor tag

The conventional RFID architecture consists of a Power Management Unit (PMU), a RFID frontend, and digital logic (Fig. 1.10). The PMU harvests the RF field energy and converts it to the DC voltage V_{DC}. Further they are regulated supply voltages V_{DD} for the chip. The rectifiers, the bandgap, and the low-dropout regulators (LDO) form the main power path. The power limiter limits the voltage when the incoming power is too high. The power-on reset (POR) circuit generates the reset signal during start-up. The RFID frontend consists of a demodulator, a modulator, and a clock recovery circuit [13, 24]. The demodulator converts the modulated RF signal to a digital bitstream "DEMOD", while the modulator modulates the response "MOD" to the carrier signal. The clock recovery module extracts the RFID carrier frequency and scales it down to a lower frequency signal "Clock" for system operation. The digital logic executes the received RFID command and modulates the response back onto the carrier wave. The digital block comprises a protocol engine and memory.

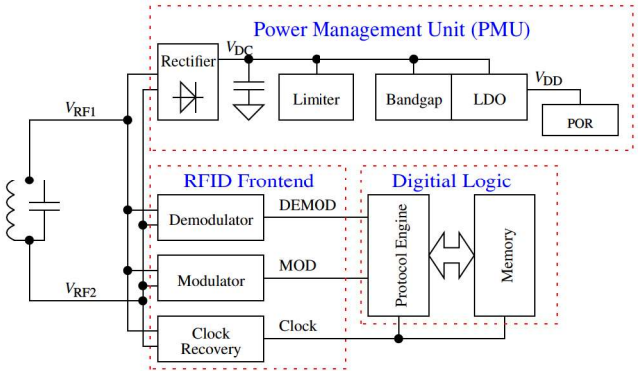


Fig. 1.10 Conventional RFID architecture utilizes three main blocks: a PMU, a frontend and a digital logic.

Battery-less sensing using RFID technology is an attractive choice for many applications requiring wireless temperature acquisition. The design challenges posed by such systems are to achieve low power, low cost, and high sensor accuracy. Many of the latest commercial/research solutions utilize the combination of RFID frontends, low-power micro-controller units (MCU) and stand-alone sensors [80, 58, 54, 50, 19]. The trade-off of such systems are the high cost, the relatively complex overall system and the relatively high power consumption.

In [80], the commercial RFID sensor chip (Fig. 1.11) integrates no on-chip temperature sensor but an on-chip $\Sigma\Delta$ ADC. The temperature sensing is accomplished with an off-chip thermistor. With several off-chip discrete components, it is difficult to miniaturize the final product size.

In contrast, state-of-the-art wireless sensor tags implement the sensor directly in the chip without using an MCU [90, 36, 43, 44, 25, 10]. This lets the sensor work in closer conjunction with the RFID functionality and allows for system performance optimization. In addition, system size and complexity can be significantly reduced to enable miniaturized low-cost applications. A

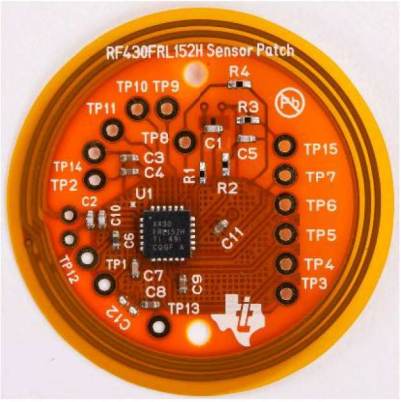


Fig. 1.11 Commercial RFID sensor tag utilizes MCU and many discrete components [80].

wireless glucose sensor [25] is implemented on a contact lens for noninvasive continuous health monitoring. A fully-integrated miniaturized wireless neural sensor [10] is realized for brain-machine interface applications.

In [43], the temperature sensor [23] is implemented in a UHF RFID sensor tag. The accuracy is obtained with ±0.8 °C while a sensing range is achieved from −20 °C to 30 °C. The entire conversion time takes 40 ms, so the sampling rate is 25 Samples/s.

A wireless temperature sensor [36] operating from approximately 25 °C to 45 °C with an accuracy of 0.4 °C was demonstrated. The simplified block diagram of the temperature sensor is shown in Fig. 1.12. The voltage V_{Temp} is obtained in a bias core. Then V_{Temp} is converted into a clock signal in a relaxation oscillator, whose frequency is temperature dependent. The design utilizes no communication protocol, but modulates the clock frequency directly to the carrier frequency. The design complexity is significantly reduced, while the chip is no longer compatible to the commercial readers.

In [44], a RFID temperature sensor, which utilizes bipolar core and ΣΔ ADC, achieves an accuracy of $[-1, 0.8]$ °C from −20 °C to 50 °C.

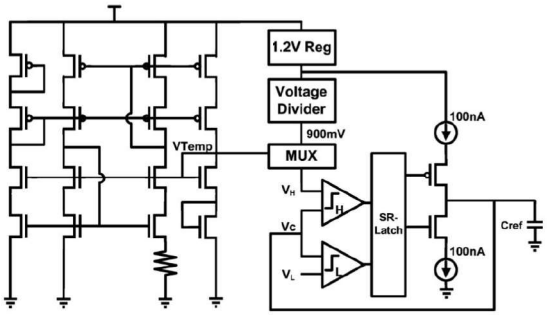


Fig. 1.12 Block diagram of the temperature sensor in [36].

Supply noise introduction

Every sensor utilizes one voltage as power supply. An ideal supply voltage can be regarded as a stable and noise-free DC voltage with unlimited current drive capability. For the stand-alone sensor, this ideal power supply could be approximately given. However, if the sensor is integrated with other components in a system-on-chip (SoC), the supply voltage is affected by all the components together. Therefore, due to the non-ideal supply voltage, the sensor's performance could be degraded.

Many state-of-the-art papers discussed the impacts of supply noise in different application scenarios. When designing a Wheatstone bridge [41], a typical resistive sensor consists of four resistors, amplifiers and ADC (Fig. 1.13). The resistors are supplied directly from the supply voltage. If the bridge is balanced, the supply noise will not generate any mismatch at the bridge output. However, the unbalanced bridge will output a significant error under supply mismatch. In addition, the sensor error also shows a non-linearity to the supply voltage mismatch as well, making sensor's inaccuracy compensation even more complicated.

In the phase-locked loop (PLL) design [11], the voltage-controlled oscillator (VCO) is the critical block that defines the phase noise of the output. The VCO

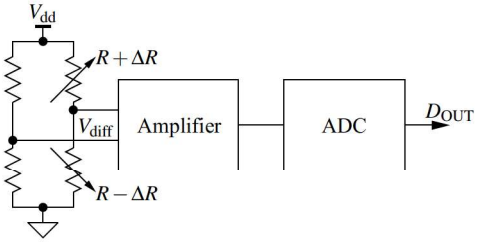


Fig. 1.13 Block diagram of a typical Wheatstone bridge sensor element.

is usually built by inverter-based ring oscillators, which provide the simple and small chip area solutions unlike *LC* tank VCOs. However, this structure suffers a high supply noise sensitivity and high noise floor.

To overcome this problem of supply noise, different papers utilize different strategies. In [11, 15], the PLL introduces a local regulation with dedicated tuning scheme to filter out the supply noise. In [41], the researchers present a force-balanced Wheatstone bridge interface circuit with highly improved overall PSRR and temperature resilience in one circuit. On the other hand, inside a SoC the noise can be reduced directly from the source. The power management units (PMUs) are optimized to provide less-noisy supplies [8, 14, 17].

1.4 Task definition and proposal of this thesis

Table 1.1 shows a representative specification of such a sensor unit. In particular, the combination of requirements in terms of dimensions, power consumption and sampling speed poses a high challenge which will be addressed in this thesis. Please notice that the pH sensor is not in the scope of this work.

In this thesis, the design methodology and implementation of fully passive RFID temperature sensor SoC are proposed. To overcome the issues of low accuracy and small operational range for RFID temperature sensors, new ideas have been made in this dissertation.

Table 1.1 Representative specification of a wireless micro-sensor [62]

Parameter	Target value	Vision
Physical, electrochemical measurements	Temperature, pH value	Temperature, pH value Pressure,...
Accuracy of temperature measurements	±0.25 °C (10 °C to 40 °C) ±0.5 °C (0 °C to 70 °C)	±0.1 °C (10 °C to 40 °C) ±0.25 °C (0 °C to 70 °C)
Accuracy of pH measurements	±0.1 pH (10 °C to 40 °C)	±0.05 pH (10 °C to 40 °C)
Power consumption of the sensor	<100 µW	<10 µW
Supply voltage of the sensor	<3 V	<1 V
Sampling rate	>10 Samples/s	>100 Samples/s
Chip area	<2 mm^2	<1 mm^2

First of all, a novel *time-domain temperature sensor topology* [87, 85] is developed in order to achieve high-accuracy and low-power at same time. The experimental results shows that this temperature sensor achieves $[-0.1, 0.5]$ °C from –40 °C to 125 °C, which is the best-in-class performance among the low-power time-domain temperature sensors.

Besides that, since the supply interference is the largest difference between stand-alone and RFID temperature sensors, a complete *methodology* [86, 89, 88, 92, 91] is developed to analyze the generation, the amplification and the digitization of the supply interference. This design methodology is considered as the most significant scientific contribution of this dissertation.

The analysis results show that this new topology provides the least DC interference sensitivity among the current time-domain temperature sensor topologies, while it still suffers from high AC interference sensitivity. To solve this issue a *system level optimization* [90, 89] is achieved by adding a new RFID

command, which can bypass the noisy sensor data but output only the less-noisy ones.

The experimental results [90] show that this proposed RFID temperature sensor achieves ±0.4 °C (3σ) from 0 °C to 125 °C, which is the highest accuracy with the widest operational range in comparison with currently reported state-of-the-art RFID temperature sensors. The sampling rate is achieved with 676 Samples/s. The new RFID command improves the noise performance of this RFID temperature sensor by a factor of 16.

1.5 Structure of this thesis

This thesis is organized as follows:

Chapter 2, Design methodology of supply noise analysis. The behaviour of the supply noise is analysed in this chapter. The chapter begins with the generation of the supply noise. Then the supply noise is passed through the power management unit and reaches the sensor, affecting the sensor performance. To systematically analyze the supply noise, this chapter utilizes the methodology of modeling, transfer function calculation, verification and comparison.

Chapter 3, Mixed-signal circuit implementation. The circuit implementation also introduces many challenges, due to the process, voltage and temperature (PVT) variations. This chapter presents the detailed implementation of the low-power time-domain temperature sensor and the RFID. The temperature sensor is built on an individual test chip, whose experimental results are also presented in this chapter.

Chapter 4, System integration and physical design. Because of the supply interference, the system level optimization on the RFID communication is achieved by introducing a new RFID command. Finally, the top-level schematic

and the layout are shown.

Chapter 5, Experimental results. This chapter shows the characterization results of this proposed RFID temperature sensor and compares it with the state-of-the-art works.

Chapter 6, Summary and outlook. This concluding chapter discusses how the insights developed in this thesis can be put into future RFID sensor designs.

Chapter 2

Design methodology of supply noise analysis

2.1 Introduction

In order to achieve a low-power high-precision temperature sensing in a RFID SoC, a lot of design concepts can be used. With V-diagram approach, the designer can systematically research the crucial design challenges. And the design space is narrowed down, so that the design goals can be achieved more efficiently. The new chip architecture can be established, if the design constrains can be satisfied.

The basic RFID block diagram is already shown in Fig. 1.10. Since RFID needs to cooperate with sensors, the topology needs to be improved. In Fig. 2.1, an additional supply path is added so that the analog blocks are supplied by V_{DDA}, which is different from the digital blocks. The advantage of this configuration is that the supply noise, which is generated by digital circuits, is not be transmitted directly to the analog circuit. The communication with the sensor

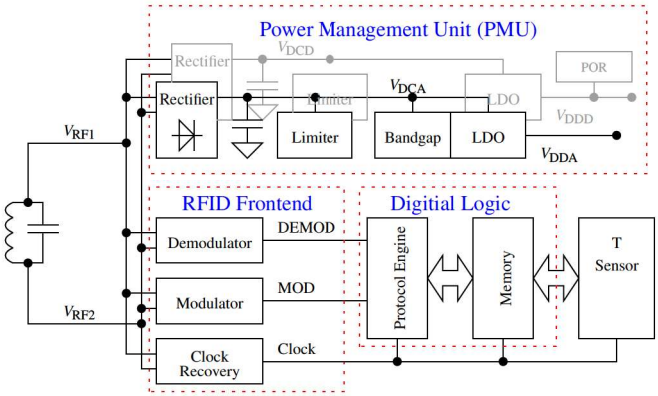


Fig. 2.1 This improved PMU consists of two supply paths and a sensor interface.

is realized by placing the sensor interface in the memory. Thus, the sensor can be controlled and readout by simple RFID write and read commands.

Many RFID sensors suffer low accuracy and small sensing range [36, 43, 44], since the sensors are not only affected by their own noise. The noise from the supply path had a much greater impact on the sensor performance.

In Fig. 2.2, the design space is narrowed down to three challenges.

The first challenge is the noise generation, which is related to the RFID functionality. Since the RFID communication is modulated on the RF field, the amplitude changing of the RF field strength can be seen as a dynamic noise. This noise is rectified and added to the unregulated DC voltage V_{DCA} (Fig. 2.2 ①) in PMU. The second challenge is the noise amplification within PMU (Fig. 2.2 ②). The PMU converts the DC unregulated voltage V_{DCA} into a DC regulated voltage V_{DDA}. The supply noise on the regulated supply voltage in state-of-the-art RFID designs exists widely. In [53], it can be seen that approximately 100 mV ripple is generated on a 0.5 V supply during communication. In [90], a 540 mV peak-to-peak AC ripple is measured on a 1.2 V analog supply. The final challenge is the noise digitization from the analog supply voltage to the digital output via the temperature sensor (Fig. 2.2 ③). This results in low sensor accuracy

and small sensing range. This effect is observed in [7], but was barely discussed in the paper. Therefore, the analysis of the effects of the supply on the temperature sensors is essential.

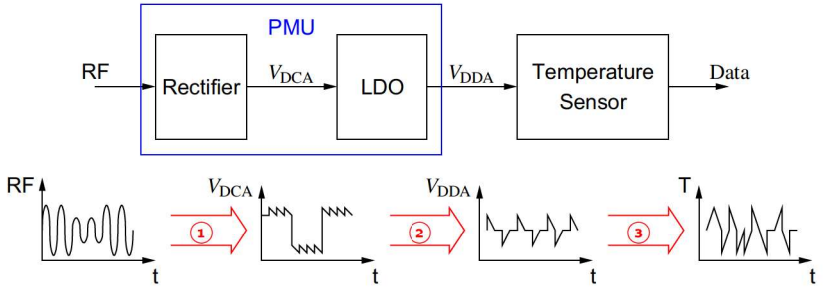


Fig. 2.2 The design space is narrowed down into three challenges, which include ①: noise generation, ②: noise amplification and ③: noise digitization.

In Fig. 2.2 ②, the noise amplification can be described by power supply rejection (PSR), which is the supply-to-output characteristic in the frequency domain. Many state-of-the-art designs [8, 14, 17, 48, 45] utilize PSR analysis and optimization of their proposed structures. The analysis of transfer functions went so deep that the parasitic effects are present in their equations. However, their design methodologies, which explain their design trade-offs, are normally not presented and compared. Another problem is that their designs could be dependent on CMOS technology and under certain trade-offs, e.g. input/output range, power consumption, speed or design complexity. As a result, their design techniques could not easily be implemented for daily designs.

In this chapter, the three challenges, namely noise generation, noise amplification and noise digitization, are analyzed and discussed. The noise generation is described and analyzed from different sources in the frequency domain. The noise amplification is investigated by modeling of a typical PMU block. A common approach is presented to analyze and optimize the system behaviour for the crucial component of PMU, namely low-dropout regulator (LDO). The comparison of PSR between transistor design and modeling is demonstrated.

With the modeling, the system behaviour can be explained. The investigation of noise digitization requires a model of the temperature sensor. In this thesis, a novel time-domain low-voltage low-power CMOS on-chip temperature sensor topology for a temperature range from −40 °C to 125 °C is presented. The sensor topology is based on a delay circuit that generates a PWM signal from diode-connected BJTs. The duty cycle of the delay signal is proportional to the absolute temperature. In order to evaluate the noise digitization of different temperature sensors, models of various state-of-the-art temperature sensors are built. All models are built in the same technology, so that the models represent the realistic CMOS circuit. The comparison of the noise sensitivity of the sensor models uncovers the most robust sensor topology, which suffers least from supply noise.

This chapter is organized as follows. In section II, the supply noise generation in the typical RFID architecture is presented. The noise amplification is modeled, simulated and discussed in section III. Section IV describes the concept of the time-domain temperature sensor. The modeling and comparison of noise digitization are explained in section V. Finally, conclusions are drawn in section VI.

2.2 Generation of the supply noise

The ripple can be generated from three different sources [91].

Ripple from RF carrier

Firstly, the RF carrier brings a significant ripple to V_{DCA} and V_{DCD} even after the AC signal is rectified in Fig. 2.1. In Fig. 2.3 (a) a typical V_{DC} is shown that the ripple oscillates between 2.3 V and 2.45 V. This is because the smoothing capacitors on the output of the rectifier (Fig. 2.1) are normally not large enough, since the smoothing capacitors are built on the chip. In the frequency domain the spectrum of V_{DC} (Fig. 2.3 (b)) shows that the signal is concentrated

on 27.12 MHz and its harmonics. 27.12 MHz is twice as high as the RF carrier frequency (13.56 MHz), because the modern rectifiers are full wave rectifiers that charge the load twice in a cycle.

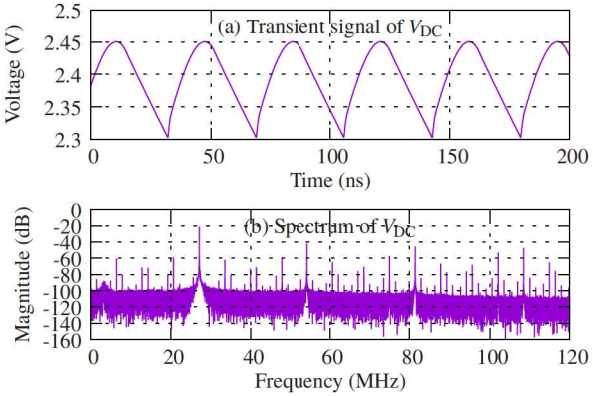


Fig. 2.3 (a) The transient signal of a typical V_{DC} and (b) its spectrum.

Ripple from RFID communication

Besides that, the communication between reader and tag is realized by digital modulation Amplitude Shift Keying (ASK), which modulates the amplitude on the RF carrier. The modulation depth of V_{AC} is typically defined with 0 % and 80 % for IEC/ISO 14443 Type A and Type B [73], respectively. In Fig. 2.4 (a), the reader-to-tag communication (left side) and tag-to-reader communication (right side) utilize 106 kHz and 848 kHz, respectively. Due to the amplitude modulation, the rectifier output V_{DC} in Fig. 2.4 (b) generates significant voltage drops, since the load constantly draws current from the smoothing cap. The voltage drops are dependent on the load, the smoothing cap and the rectifier output resistance. In Fig. 2.4 (c), the spikes happen exactly at 106 kHz and its harmonics. Since the tag responses (106 kHz) are modulated on a 848 kHz subcarrier frequency according to the protocol, the spectrum of the response signal

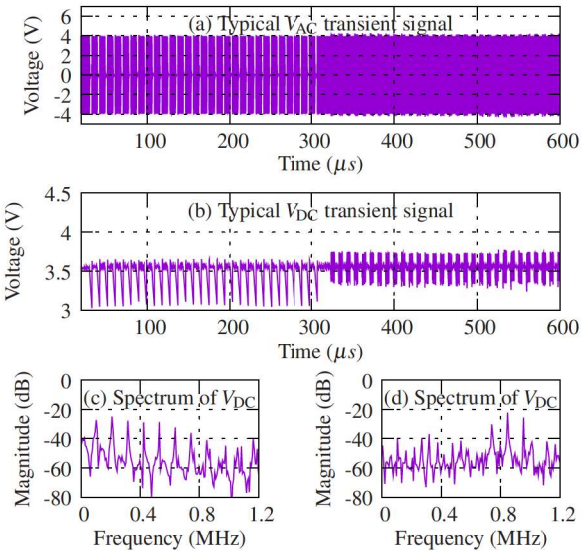


Fig. 2.4 (a) A typical RF transmission waveform V_{AC} with reader-to-tag communication (left) and tag-to-reader communication (right) and (b) the corresponding rectified voltage V_{DC} with the spectrum of V_{DC} for (c) reader-to-tag communication and (d) tag-to-reader communication

in Fig. 2.4 (d) clearly shows three spikes at 742 kHz, 848 kHz and 954 kHz. In General, the communication ripples are approximately distributed between 100 kHz and 1 MHz.

Ripple from incoming power and the load

At the end, the DC level of V_{DCA} and V_{DCD} is determined by the incoming power and load, namely reader output power, geometry and system power consumption. The induced voltage changing is basically in the low-frequency band, due to the fact that geometry and load condition change relatively slowly.

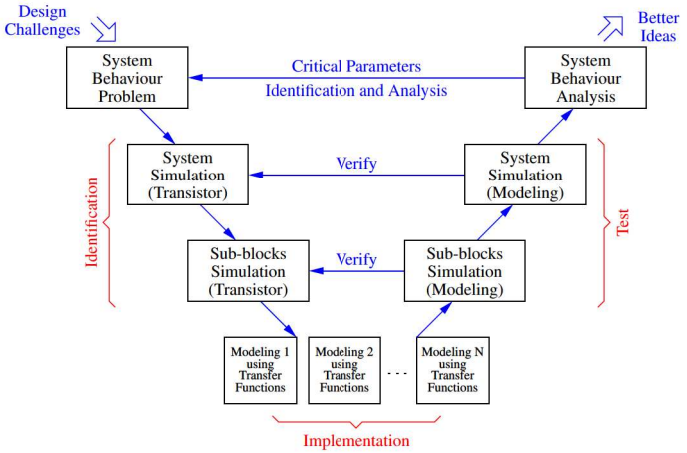


Fig. 2.5 Using V-diagram to systematically analyze the amplification of the supply noise

2.3 Amplification of the supply noise

From the block diagram in Fig. 2.1, the interference can pass to the analog supply voltage V_{DDA} on two paths. Firstly, the interference on V_{DCA} is directly applied to the LDO. The second path comes from the bandgap voltage reference, which provides the reference voltage for the LDO.

Among the three independent processes, the amplification of the supply noise is the most important, but is also difficult to analyse. The challenge is: How can the critical design aspects for the system behaviour problem be found efficiently and rapidly? In this case, the problem is to analyse the conducted ripple from the rectifier output to the sensor input. Based on the V-diagram introduced in Chapter 1, the entire process can be divided into three sub-processes.

Firstly, the problem must be identified. Since this problem has already been shown in various works, it should not be difficult to recreate the failure scenario. The power signal V_{DCA} in Fig. 2.2 is passed directly to the LDO. The LDO should be analyzed in any case. However, another hidden path can also affect

the LDO output. In Fig. 2.1, the bandgap reference takes V_{DCA} as supply voltage and outputs the reference voltage used by the LDO. Therefore, the bandgap and the LDO must be analyzed together.

The second step is to implement the modeling, which simplifies the analysis of the circuit. The transistor-level circuit contains too much information, which is sometimes difficult to separate the critical parameters and the non-critical ones. The modeling captures the essential properties of a transistor-level circuit, so that the critical parameters can be extracted directly from these essential properties. The way the modeling is built can be decided by the designer.

The final step is to verify the modeling by comparing the the simulation results of the modeling to the simulation results of the transistor circuit. The modeling of the sub-blocks must first be verified, until the simulation results of the transistor circuit and the modeling are matched. The system modeling is then built from the sub-block models. The modeling should be trimmed until the modeling reveals the problem exactly.

With modeling, the critical parameters that dominate the problem can analyzed much more easily. Thus, the key for solving the problem can be easily found and new ideas for improvement can be developed.

2.3.1 Problem identification

The PSR is defined as the gain from the input supply signal to the output supply signal in the frequency domain. A typical low power PMU design is utilized to simulate for modeling. The results of the PSR simulation of a bandgap reference and an LDO are shown in Fig. 2.6.

The DC PSR curves of both the bandgap reference and the LDO are below zero with the number of −77 dB and −46 dB, respectively. This means that the DC supply noise is significantly reduced. However, if the frequency goes higher, the PSR gets worse. From 130 Hz to 75 kHz, the PSR of the bandgap reference is above 0 dB. In this frequency range, the supply noise is amplified. For LDO, the frequency range for noise amplification is between 20 kHz to 8 MHz. Un-

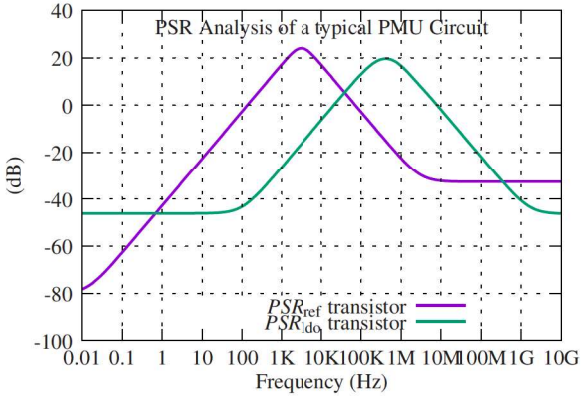


Fig. 2.6 The PSR simulations of a bandgap and an LDO in the frequency domain.

fortunately, these frequency ranges are widely used by sensor operations and RFID communication. From the simulation of PSR, the problem is identified that the PMU amplifies the supply noise in a wide frequency range.

2.3.2 Modeling implementation

The typical combination of bandgap and LDO for power analysis is shown in Fig. 2.7. On the left, the bandgap voltage reference consists of a bandgap core (Q_1, Q_2, R_1 and R_2), an error amplifier and a transistor M_1. With the feedback loop, the bandgap core is properly biased and generates the reference voltage V_{REF}. On the right, the voltage V_{REF} is passed to the LDO, which is formed by A_2, M_2, R_3 and R_4. The output regulated supply voltage V_{DDA} is generated by the LDO and supplies the load described by R_{L} and C_{L}.

In Fig. 2.8, the blocks are summarized to analyze the signal flows and the transfer function. Every block represents a single gain stage with voltage input and voltage output. Each "macro circuit" is built by the signal gain stage, e.g. A_2, and supply gain stage, e.g. PSR_2, as long as the gain stage consumes power

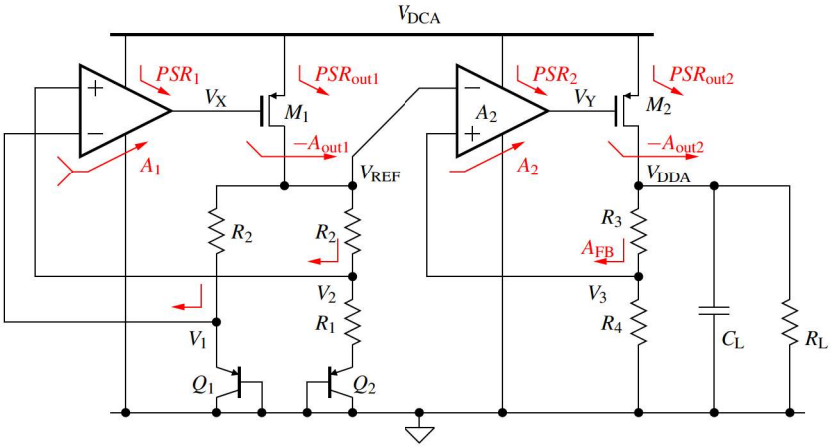


Fig. 2.7 The simplified circuit [91] combines the voltage reference and LDO for transfer function analysis.

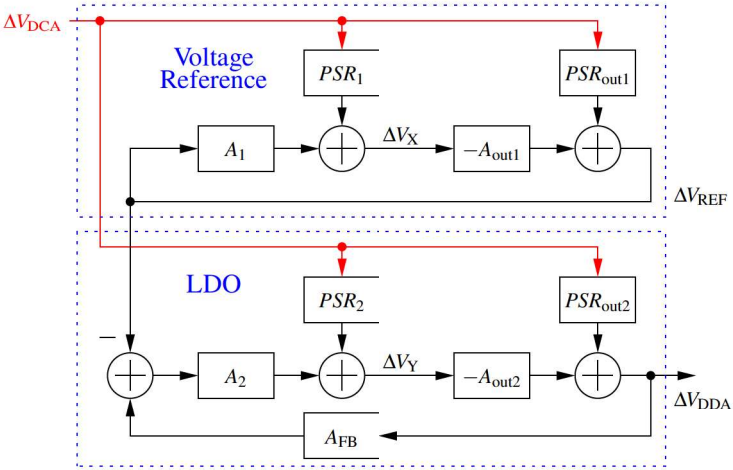


Fig. 2.8 To analyze the transfer function from ΔV_{DCA} to ΔV_{DDA}, the signal flow graph of the circuit [91] is drawn with the consideration of ΔV_{DCA}.

from supply. The signals of two gain stages are summed to generate the output signal, since the real circuit has only one output port. All blocks without A_{FB} are modeled with one pole to reveal the system behaviour without complicating the calculation. Please notice that the bandgap error amplifier and feedback are combined to a common gain stage to simplify the calculation. Table 2.1 summarizes the models for the further analysis.

Table 2.1 Summarized parameters for the further analysis

Macro circuit	Signal gain stage	Supply gain stage
Voltage reference error amplifier	$A_1 = \frac{A_{1,DC}}{1+\frac{s}{\omega_1}}$	$PSR_1 = \frac{PSR_{1,DC}}{1+\frac{s}{\omega_1}}$
Voltage reference output stage	$A_{out1} = \frac{A_{out1,DC}}{1+\frac{s}{\omega_{out1}}}$	$PSR_{out1} = \frac{PSR_{out1,DC}}{1+\frac{s}{\omega_{out1}}}$
LDO Error amplifier	$A_2 = \frac{A_{2,DC}}{1+\frac{s}{\omega_2}}$	$PSR_2 = \frac{PSR_{2,DC}}{1+\frac{s}{\omega_2}}$
LDO Output stage	$A_{out2} = \frac{A_{out2,DC}}{1+\frac{s}{\omega_{out2}}}$	$PSR_{out2} = \frac{PSR_{out2,DC}}{1+\frac{s}{\omega_{out2}}}$

2.3.3 Transfer function calculation

In Fig. 2.8, the system behaviours can be written as:

$$\Delta V_X = \Delta V_{REF} A_1 + \Delta V_{DCA} PSR_1, \tag{2.1}$$

$$\Delta V_{REF} = -\Delta V_X A_{out1} + \Delta V_{DCA} PSR_{out1}, \tag{2.2}$$

$$\Delta V_Y = (\Delta V_{DDA} A_{FB} - \Delta V_{REF}) A_2 + \Delta V_{DCA} PSR_2, \tag{2.3}$$

$$\Delta V_{DDA} = -\Delta V_Y A_{out2} + \Delta V_{DCA} PSR_{out2}. \tag{2.4}$$

The equations from (2.1) to (2.4) can be simplified as:

$$\Delta V_{\mathrm{DDA}} = \frac{PSR_{\mathrm{out2}} - A_{\mathrm{out2}} PSR_2}{1 + A_2 A_{\mathrm{FB}} A_{\mathrm{out2}}} \Delta V_{\mathrm{DCA}} + \frac{A_2 A_{\mathrm{out2}}}{1 + A_2 A_{\mathrm{FB}} A_{\mathrm{out2}}} \Delta V_{\mathrm{REF}}, \tag{2.5}$$

$$\Delta V_{\mathrm{REF}} = \frac{PSR_{\mathrm{out1}} - A_{\mathrm{out1}} PSR_1}{1 + A_1 A_{\mathrm{out1}}} \Delta V_{\mathrm{DCA}}. \tag{2.6}$$

The PSR from input supply changing ΔV_{DCA} to output signal changing ΔV_{DDA} can be expressed as:

$$PSR = \frac{\Delta V_{\mathrm{DDA}}}{\Delta V_{\mathrm{DCA}}}, \tag{2.7}$$

$$= PSR_{\mathrm{ldo}} + A_{\mathrm{cl,ldo}} \cdot PSR_{\mathrm{ref}}, \tag{2.8}$$

$$= \underbrace{\frac{PSR_{\mathrm{out2}} - A_{\mathrm{out2}} PSR_2}{1 + A_2 A_{\mathrm{FB}} A_{\mathrm{out2}}}}_{1} + \underbrace{\frac{A_2 A_{\mathrm{out2}}}{1 + A_2 A_{\mathrm{FB}} A_{\mathrm{out2}}}}_{2} \cdot \underbrace{\frac{PSR_{\mathrm{out1}} - A_{\mathrm{out1}} PSR_1}{1 + A_1 A_{\mathrm{out1}}}}_{3}. \tag{2.9}$$

The equation (2.9) has three terms. The term 1 PSR_{ldo} is PSR of LDO, which is only dependent on the LDO itself. The second term $A_{\mathrm{cl,ldo}}$ indicates the closed-loop gain of the LDO, which is approximately $1/A_{\mathrm{FB}}$ at DC. he term 3 PSR_{ref} is contributed by the PSR of the bandgap. The product of term 2 and term 3 means that the PSR of the bandgap voltage reference is amplified by the LDO.

PSR of the LDO PSR_{ldo}

In Fig. 2.7, A_{out2} can be seen as common-source stage, while PSR_{out2} can be understood as common-gate stage. The DC gain of A_{out2} and PSR_{out2} can be expressed by:

$$A_{\mathrm{out2,DC}} = g_{\mathrm{m2}} r_{\mathrm{out}}, \tag{2.10}$$

$$PSR_{\mathrm{out2,DC}} = (g_{\mathrm{m2}} + g_{\mathrm{ds2}}) r_{\mathrm{out}}, \tag{2.11}$$

where g_{m2} and g_{ds2} are the small-signal transconductance of gate-source voltage and drain-source voltage, r_{out} is the output resistance. Since $g_{ds2} \ll g_{m2}$, $A_{out2,DC}$ is approximately same as $PSR_{out2,DC}$.

Combing the equations of Table 2.1, PSR_{ldo} of the equation (2.9) can be written as [92]:

$$PSR_{ldo} = \frac{(-A_{out2,DC}PSR_{2,DC}\omega_2 - PSR_{out2,DC}(s+\omega_2))\omega_{out2}}{(s+\omega_2)(s+\omega_{out2}) + A_{2,DC}A_{FB}A_{out2,DC}\omega_2\omega_{out2}}, \tag{2.12}$$

$$= PSR_{ldo,DC}\frac{1+\frac{s}{z_2}}{(1+\frac{s}{p_{2,1}})(1+\frac{s}{p_{2,2}})}. \tag{2.13}$$

The equation (2.13) shows two poles and one zero, so that the position of zero and poles needs to be analyzed in order to reveal the system behaviour.

The DC gain of PSR_{ldo} can be expressed by:

$$PSR_{ldo,DC} \approx \left| \frac{PSR_{out2,DC}}{A_{out2,DC}} - PSR_{2,DC} \right| \frac{1}{A_{2,DC}A_{FB}}, \tag{2.14}$$

$$\approx |1 - PSR_{2,DC}| \frac{1}{A_{2,DC}A_{FB}}. \tag{2.15}$$

$$\downarrow 1 \qquad \downarrow 2$$

Two terms are presented in equation (2.15). The term 2 defines the fundamental value, which comes from the error amplifier and feed back. More DC gain of the error amplifier generates enhanced DC PSR (more DC noise reduction). The term 1, which is dependent on $PSR_{2,DC}$, is a factor that amplifies the fundamental value. By making $PSR_{2,DC}$ as close as 1 ($PSR_{out2,DC}/A_{out2,DC}$), the DC PSR can be significantly reduced.

The zero of equation (2.13) can be written as:

$$z_2 \approx \left| 1 - \frac{A_{out2,DC}PSR_{2,DC}}{PSR_{out2,DC}} \right| \omega_2, \tag{2.16}$$

$$\approx |1 - PSR_{2,DC}| \omega_2. \tag{2.17}$$

$$\downarrow 1 \qquad \downarrow 2$$

The term 2 of equation (2.17) is linked to the 3 dB frequency of the error amplifier (ω_2). More bandwidth of the error amplifier results in higher frequency of the zero. The term 2 is again amplified by a factor (term 1), which is similar as term 1 in equation (2.15).

By calculating $z_2/PSR_{\text{ldo,DC}}$, a bandwidth (BW) can be obtained:

$$BW = \frac{z_2}{PSR_{\text{ldo,DC}}} \approx \frac{A_{\text{out2,DC}} A_{\text{2,DC}} A_{\text{FB}}}{PSR_{\text{out2,DC}}} \omega_2, \tag{2.18}$$

$$\approx A_{\text{2,DC}} A_{\text{FB}} \omega_2. \tag{2.19}$$

It can be seen that the zero and DC PSR are dependent on $PSR_{\text{2,DC}}$, while their ratio is independent of it. In the Bode diagram (Fig. 2.9), the movement of zero starts with $PSR_{\text{2,DC}} = 0$ (①). As $PSR_{\text{2,DC}}$ increases and moves toward 1, the DC PSR reduces, while the zero moves to the lower frequency (②). If $PSR_{\text{2,DC}}$ is larger than 1 and continues to rise, the corner turns back, so that DC PSR increases and zero moves to a higher frequency (③). When $PSR_{\text{2,DC}}$ is near $A_{\text{2,DC}} A_{\text{FB}}$ (④), the DC PSR becomes 0 dB, while the zero becomes BW ($A_{\text{2,DC}} A_{\text{FB}} \omega_2$).

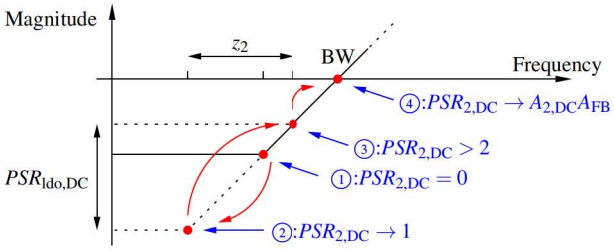


Fig. 2.9 The zero and DC PSR move as $PSR_{\text{2,DC}}$ increases from 0 to $A_{\text{2,DC}} A_{\text{FB}}$.

The two poles of LDO PSR can be calculated as:

$$p_{2,1} = \frac{1}{2}\left(\omega_2 + \omega_{out2} + \sqrt{(\omega_2 - \omega_{out2})^2 - 4A_{ol2,DC}\omega_2\omega_{out2}}\right), \tag{2.20}$$

$$p_{2,2} = \frac{1}{2}\left(\omega_2 + \omega_{out2} - \sqrt{(\omega_2 - \omega_{out2})^2 - 4A_{ol2,DC}\omega_2\omega_{out2}}\right). \tag{2.21}$$

If $(\omega_2 - \omega_{out2})^2 - 4A_{ol2,DC}\omega_2\omega_{out2} > 0$, the resulted poles are real. Otherwise the poles are complex conjugate pairs, which will generate a magnitude spike on the frequency response in the bode plot.

If the poles are real, they are mirrored by the central point of $\frac{1}{2}(\omega_2 + \omega_{out2})$. Their distance to the central point is defined by the ratio $R = \frac{\omega_{out2}}{\omega_2}$. The more the ratio is, the more distance they have. The poles in Fig. 2.10 are limited by:

$$p_{2,2,min} = \lim_{R\to\infty} p_{2,2} \approx A_{ol2,DC}\omega_2, \tag{2.22}$$

$$p_{2,1,max} = \lim_{R\to\infty} p_{2,1} \approx \omega_{out2}. \tag{2.23}$$

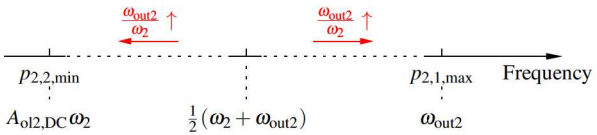


Fig. 2.10 The real poles are mirrored by $\frac{1}{2}(\omega_2 + \omega_{out2})$

The theoretical peak PSR can be obtained in two cases.

If the zero is the smallest among the zero and poles. The magnitude of the frequency response increases after the zero and reaches the maximum between two poles. The theoretical peak PSR (Fig. 2.11) occurs only when the two poles are far away from each other, i.e., $p_{2,1} \ll p_{2,2}$. In this case the peak PSR can be

calculated by:

$$PSR_{\mathrm{ldo,peak}} = PSR_{\mathrm{ldo,DC}} \frac{1+\frac{f_{\mathrm{ldo,peak}}}{z_2}}{(1+\frac{f_{\mathrm{ldo,peak}}}{p_{2,1,\max}})(1+\frac{f_{\mathrm{ldo,peak}}}{p_{2,2,\min}})}, \tag{2.24}$$

$$\approx PSR_{\mathrm{ldo,DC}} \frac{\frac{f_{\mathrm{ldo,peak}}}{z_2}}{1 \cdot \frac{f_{\mathrm{ldo,peak}}}{p_{2,2,\min}}}, \tag{2.25}$$

$$\approx PSR_{\mathrm{ldo,DC}} \frac{p_{2,2,\min}}{z_2}, \tag{2.26}$$

$$= \frac{\left| \frac{PSR_{\mathrm{out2,DC}}}{A_{\mathrm{out2,DC}}} - PSR_{2,\mathrm{DC}} \right|}{A_{2,\mathrm{DC}} A_{\mathrm{FB}}} \frac{A_{\mathrm{ol2,DC}}\omega_2}{\left| 1 - \frac{A_{\mathrm{out2,DC}} PSR_{2,\mathrm{DC}}}{PSR_{\mathrm{out2,DC}}} \right| \omega_2}, \tag{2.27}$$

$$= \frac{\left(-PSR_{2,\mathrm{DC}} + \frac{PSR_{\mathrm{out2,DC}}}{A_{\mathrm{out2,DC}}} \right)}{A_{2,\mathrm{DC}} A_{\mathrm{FB}}} \cdot \frac{A_{2,\mathrm{DC}} A_{\mathrm{FB}} A_{\mathrm{out2,DC}} \omega_2}{\left(1 - \frac{A_{\mathrm{out2,DC}} PSR_{2,\mathrm{DC}}}{PSR_{\mathrm{out2,DC}}} \right) \omega_2}, \tag{2.28}$$

$$= PSR_{\mathrm{out2,DC}}. \tag{2.29}$$

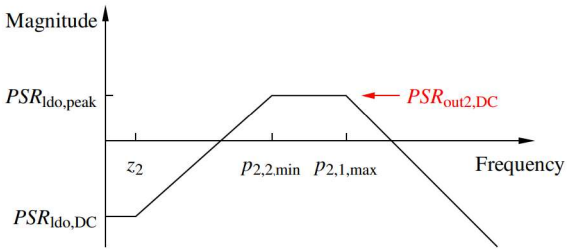


Fig. 2.11 The theoretical peak PSR is obtained when the two poles are far away from each other, so that a flat region is created between the poles.

If one pole is the smallest among the zero and poles. In this case the DC PSR is the peak PSR, since the magnitude doesn't increase any more.

$$PSR_{\text{ldo,peak}} = PSR_{\text{ldo,DC}} = \left| \frac{PSR_{\text{out2,DC}}}{A_{\text{out2,DC}}} - PSR_{\text{2,DC}} \right| \frac{1}{A_{\text{2,DC}} A_{\text{FB}}}. \tag{2.30}$$

Closed-loop gain of the LDO $A_{\text{cl,ldo}}$

The closed-loop gain of the LDO is expressed by:

$$A_{\text{cl,ldo}} = \frac{A_2 A_{\text{out2}}}{1 + A_2 A_{\text{FB}} A_{\text{out2}}}, \tag{2.31}$$

$$= \frac{A_{\text{2,DC}} A_{\text{out2,DC}} \omega_2 \omega_{\text{out2}}}{(s+\omega_2)(s+\omega_{\text{out2}}) + A_{\text{2,DC}} A_{\text{FB}} A_{\text{out2,DC}} \omega_2 \omega_{\text{out2}}}. \tag{2.32}$$

Assuming $A_{\text{2,DC}} A_{\text{out2,DC}} \gg 1$, the DC closed-loop gain is approximately $1/A_{\text{FB}}$. The closed-loop gain has two poles:

$$p_{2,1} = \frac{1}{2}\left(\omega_2 + \omega_{\text{out2}} + \sqrt{(\omega_2 - \omega_{\text{out2}})^2 - 4A_{\text{ol2,DC}} \omega_2 \omega_{\text{out2}}} \right), \tag{2.33}$$

$$p_{2,2} = \frac{1}{2}\left(\omega_2 + \omega_{\text{out2}} - \sqrt{(\omega_2 - \omega_{\text{out2}})^2 - 4A_{\text{ol2,DC}} \omega_2 \omega_{\text{out2}}} \right). \tag{2.34}$$

It can be seen that the poles are the same as equations (2.20) and (2.21).

PSR of the voltage reference PSR_{ref}

In Fig. 2.8 it can be noticed that the voltage reference shares a similarity with LDO in the block structure. The calculation of the bandgap reference can be

directly given as:

$$PSR_{\text{ref}} = \frac{(A_{\text{out1,DC}} PSR_{\text{1,DC}} \omega_{\text{l}} + PSR_{\text{out1,DC}}(s+\omega_{\text{l}}))\omega_{\text{out1}}}{(s+\omega_{\text{l}})(s+\omega_{\text{out1}}) + A_{\text{1,DC}} A_{\text{out1,DC}} \omega_{\text{l}} \omega_{\text{out1}}}, \tag{2.35}$$

$$= PSR_{\text{ref,DC}} \frac{1+\frac{s}{z_1}}{(1+\frac{s}{p_{1,1}})(1+\frac{s}{p_{1,2}})}, \tag{2.36}$$

$$PSR_{\text{ref,DC}} \approx |1 - PSR_{\text{1,DC}}| \frac{1}{A_{\text{1,DC}}}, \tag{2.37}$$

$$z_1 \approx |1 - PSR_{\text{1,DC}}| \, \omega_{\text{l}}, \tag{2.38}$$

$$p_{1,1} = \frac{1}{2}\left(\omega_{\text{l}} + \omega_{\text{out1}} + \sqrt{(\omega_{\text{l}} - \omega_{\text{out1}})^2 - 4A_{\text{ol1,DC}}\omega_{\text{l}}\omega_{\text{out1}}}\right), \tag{2.39}$$

$$p_{1,2} = \frac{1}{2}\left(\omega_{\text{l}} + \omega_{\text{out1}} - \sqrt{(\omega_{\text{l}} - \omega_{\text{out1}})^2 - 4A_{\text{ol1,DC}}\omega_{\text{l}}\omega_{\text{out1}}}\right). \tag{2.40}$$

2.3.4 Modeling verification

To verify the theory, the model is simulated in comparison to the previous transistor-level low-power PMU design. The parameters listed in Table 2.2 are simply extracted from the sub-blocks of a conventional bandgap and LDO design. The aim is to check whether the PSR simulations are agreed between the transistor top level and the modeling, which utilizes the parameters of the analog sub-blocks. under this circumstance, the value of each parameter is irrelevant.

Verified by "Analog Insydes" [60], the PSR transfer function of model and transistor-level design agree to each other. The PSR characterization can be

Table 2.2 Extracted parameters of a typical low-power PMU design [92]

Parameter	Extracted value	Parameter	Extracted value
$A_{\text{out2,DC}}$	9.33 (19.3 dB)	$A_{\text{2,DC}}$	47.62 (33.6 dB)
$PSR_{\text{out2,DC}}$	9.57 (19.6 dB)	$PSR_{\text{2,DC}}$	0.79 (−2 dB)
f_{out2} ($\omega_{\text{out2}}/2\pi$)	887 kHz	f_2 ($\omega_2/2\pi$)	445 Hz
A_{FB}	1 (0 dB)	$A_{\text{ol2,DC}}$	444.29 (52.9 dB)
$A_{\text{out1,DC}}$	16.58 (24.4 dB)	$A_{\text{1,DC}}$	21.66 (26.7 dB)
$PSR_{\text{out1,DC}}$	16.62 (24.4 dB)	$PSR_{\text{1,DC}}$	1 (0 dB)
f_{out1} ($\omega_{\text{out1}}/2\pi$)	4.47 kHz	f_1 ($\omega_1/2\pi$)	5.88 Hz
		$A_{\text{ol1,DC}}$	359.12 (51.1 dB)

expressed by:

$$PSR_{\text{ldo,DC}} = 0.00494 = -46\,\text{dB}, \tag{2.41}$$

$$z_2 = 102\,\text{Hz}, \tag{2.42}$$

$$p_{2,1} = 589068\,\text{Hz}, \tag{2.43}$$

$$p_{2,2} = 298377\,\text{Hz}, \tag{2.44}$$

$$PSR_{\text{ref,DC}} = 0.000145 = -77\,\text{dB}, \tag{2.45}$$

$$z_1 = 14.15\,\text{mHz}, \tag{2.46}$$

$$p_{1,1} = 2237 + 1497\text{i}\ \text{Hz}, \tag{2.47}$$

$$p_{1,2} = 2237 - 1497\text{i}\ \text{Hz}. \tag{2.48}$$

In Fig. 2.12 the simulation results of the circuit and the model are compared. All three key parameters, namely PSR_{ldo}, PSR_{ref} and $A_{\text{cl,ldo}}$, are simulated from 10 mHz to 10 GHz.

From 10 Hz to 1 GHz, the two curves of PSR_{ldo} are relative close. From 1 GHz, the PSR of the model drops continuously with the slope of −20 dB/Decade, while the PSR of the circuit becomes flat. The reason of this effect is the parasitic capacitor C_{DS} of the LDO pass transistor. In Fig. 2.7, with the drain-source capacitor C_{DS} of M_2 and the capacitor load C_{L}, the output voltage V_{DDA} is a frac-

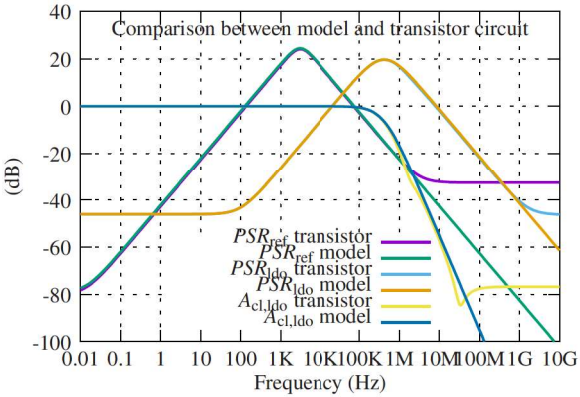


Fig. 2.12 The simulation results of a transistor-level circuit and its extracted model

tion of the input voltage V_{DCA}. The effect usually occurs in the high frequency range that is already outside the circuit's operational range.

For PSR_{ref}, the poles and zeros are lower than those of LDO, since the reference does not drive an active load, only the gate of LDO. From 10 mHz to 1 MHz, the two curves overlap. As predicted from the model and the calculation, the DC PSR reaches –77 dB, while the zero is located at 14.15 mHz. The peak PSR (≈24 dB) is reached at the poles (≈3 kHz), which are complex conjugate poles. Beyond 1 MHz the two curves drift away, due to the parasitic capacitor of the PMOS transistor (M_1 in Fig. 2.7).

Finally, the closed-loop gain $A_{\mathrm{cl,ldo}}$ remains 0 dB until the first pole. Since the two poles are close to each other, the curve bends and drops further with –40 dB. In the transistor level simulation, additional poles and zeros are shown from 1 MHz to 10 MHz, but they are insignificant, since the gain is low. If the frequency is above 30 MHz, the closed-loop gain stays flat, while the model continuously decreases. This is because the high-frequency AC signal couples directly from the input to the output. Since this effect happens in the high frequency with low gain, it is not taken into account in the modeling.

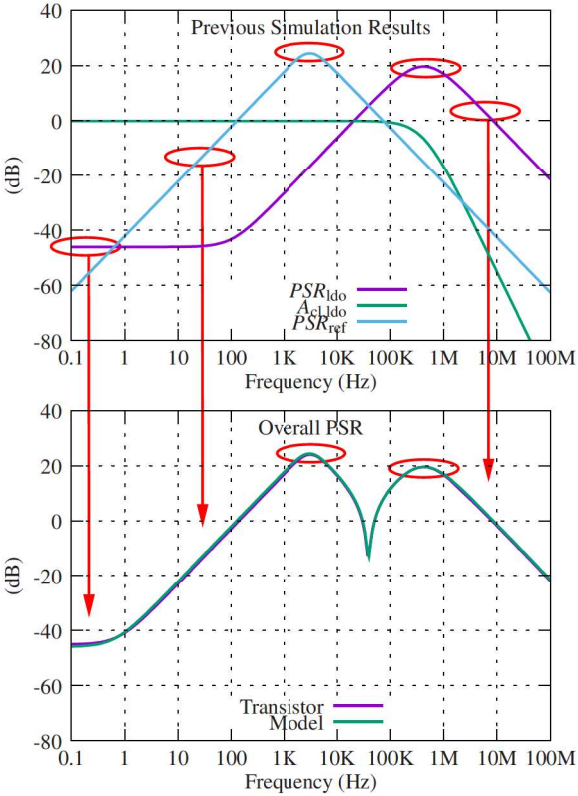


Fig. 2.13 The overall power path simulation results [91]

The combination of voltage reference and LDO can reveal the system behaviour. In Fig. 2.13, the overall PSR of the system can be divided into three areas.

- From DC to approximately 1 Hz, the system PSR follows PSR_{ldo}, since PSR_{ldo} is more significant than $A_{cl,ldo} \cdot PSR_{ref}$.

- From approximately 1 Hz to 40 kHz, the reference dominants the overall PSR, because the reference operates at a lower frequency than LDO. At approximately 3 kHz PSR_{ref} reaches its maximum value, so that the system PSR reaches this value as well.
- Beyond approximately 40 kHz, the PSR_{ldo} starts to be significant, while the overall PSR reaches another peak at approximately 400 kHz.

In Fig. 2.13, the peak PSR of the reference and LDO are approximately 24 dB and 20 dB, respectively. The peak PSR of both blocks is located between their two poles. The peak value can be written as:

$$PSR_{\text{ldo,peak}} = PSR_{\text{out2,DC}}, \tag{2.49}$$

$$PSR_{\text{ref,peak}} = PSR_{\text{out1,DC}}, \tag{2.50}$$

where $PSR_{\text{out2,DC}}$ and $PSR_{\text{out1,DC}}$ are the DC gain of PSR_{out2} and PSR_{out1} in Fig. 2.8, respectively. Since they both use PMOS transistor as pass transistor, they share the similar value.

The result shows that both reference and LDO have a significant impact on the overall performance. As long as the peak PSR is a positive value, it is unavoidable that part of the supply noise will be amplified and transferred to the noise-sensitive loads, since multiple frequencies present in such complex systems.

2.3.5 Methodology for LDO PSR optimization

As manipulating the discussed parameters, the methodology for LDO PSR optimization can be obtained. Since two different relationships of ω_2 and ω_{out2} can lead to different design strategies, it is necessary to compare the methodologies to find out the optimized design.

Desired PSR with desired bandwidth

Table 2.3 shows two strategies to achieve −50 dB PSR at 100 kHz.

Table 2.3 Design methodology comparison for PSR −50 dB@100 kHz [92]

Parameter	ω_2 dominant	ω_{out2} dominant
$A_{2,DC}$	70 dB	20 dB
$PSR_{2,DC}$	−6 dB	0.34 dB
f_2 $(\omega_2/2\pi)$	10 kHz	3.16 MHz
$A_{out2,DC}$	20 dB	20 dB
$PSR_{out2,DC}$	20.4 dB	20.4 dB
f_{out2} $(\omega_{out2}/2\pi)$	632 MHz	15.8 kHz
$PSR_{ldo,DC}$	−75 dB	−60 dB
z_2	5.2 kHz	30 kHz
$p_{2,1}$	316+316i MHz	1.59+1.59i MHz
$p_{2,2}$	316−316i MHz	1.59−1.59i MHz
Design constrains	Output stage needs high bandwidth.	Off-chip cap and dedicated $PSR_{2,DC}$ are needed.
Reference	N/A	[17, 28, 14]

The red font shows the absolute critical parameters, while the blue font and the black font represent less critical and relax parameters, respectively.

If ω_2 is set to dominant pole, $A_{2,DC}$ and f_2 are determined first, since BW is already defined by the specification.

The BW can be calculated as:

$$BW = \frac{100\,\text{kHz}}{-50\,\text{dB}} = \frac{100\,\text{kHz}}{3.16 \times 10^{-3}} = 31.6\,\text{MHz}. \tag{2.51}$$

The DC gain of the error amplifier $A_{2,DC}$ must be above 50 dB, so that the requirement of ω_2 is not crucial. Assuming $A_{FB} = 1$, from equation (2.19), the

pole of the error amplifier f_2 ($\omega_2/2\pi$) can be determined by:

$$f_2 \geq \frac{BW}{A_{FB}A_{2,DC}} = \frac{31.6\,\text{MHz}}{70\,\text{dB}}, \tag{2.52}$$

$$= 10\,\text{kHz}. \tag{2.53}$$

Since the load defines the current through the output stage, $A_{out2,DC}$ and $PSR_{out2,DC}$ are decided with 20 dB and 20.4 dB, respectively. The overall open-loop gain can be calculated as:

$$A_{ol,ldo} = A_{2,DC}A_{FB}A_{out2,DC}, \tag{2.54}$$

$$= 31620\ (90\,\text{dB}). \tag{2.55}$$

The cut-off frequency of the output stage must be high enough so that the closed-loop can remain stable.

$$f_{out2} \geq A_{ol,ldo}f_2, \tag{2.56}$$

$$\geq 316.2\,\text{MHz}. \tag{2.57}$$

In this case, f_{out2} with 632 MHz is chosen to emphasize stability. $PSR_{2,DC}$ is relative relax as long as it is below 1. It can be seen that f_{out2} (632 MHz) is relatively crucial for the implementation.

In contrast, if ω_{out2} is set to dominant pole, it should be low enough to prevent very high f_2. Assuming the error amplifier uses a simple differential pair, which has approximately 20 dB DC gain, the cut-off frequency of the error amplifier can be expressed by:

$$f_2 = \frac{BW}{A_{FB}A_{2,DC}}, \tag{2.58}$$

$$= 3.16\,\text{MHz}. \tag{2.59}$$

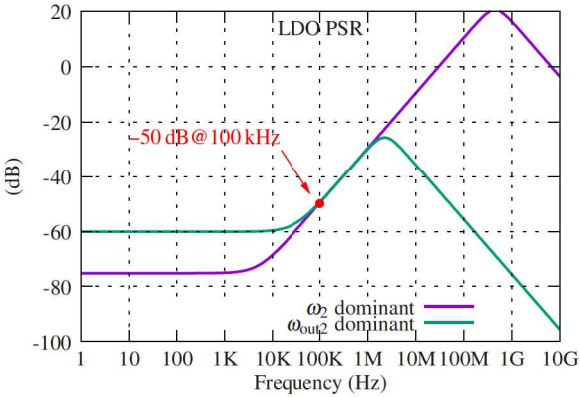


Fig. 2.14 With the parameters of Table 2.3, the simulation results show achieved PSR −50 dB@100 kHz.

The overall open-loop gain can be calculated as $A_{\text{ol,ldo}} = 100$ (40 dB). The cut-off frequency of output stage must be low enough for the closed-loop to remain stable.

$$f_{\text{out2}} \leq \frac{f_2}{A_{\text{ol,ldo}}}, \tag{2.60}$$

$$\leq 31.6\,\text{kHz}. \tag{2.61}$$

In this case, f_{out2} with 15.8 kHz is chosen to emphasize stability. Considering that the output stage usually generates a high current, an off-chip capacitor is usually required.

Table 2.4 Design methodology comparison for full-spectrum PSR −50 dB [92]

Parameter	ω_2 dominant	ω_{out2} dominant
$A_{2,DC}$	60 dB	50 dB
$PSR_{2,DC}$	−6 dB	−20 dB
f_2 ($\omega_2/2\pi$)	1 Hz	191 MHz
$A_{out2,DC}$	20 dB	20 dB
$PSR_{out2,DC}$	−50 dB	20.4 dB
f_{out2} ($\omega_{out2}/2\pi$)	42 kHz	15 kHz
$PSR_{ldo,DC}$	−66 dB	−50.5 dB
z_2	1.6 kHz	172.8 MHz
$p_{2,1}$	16.4 kHz	103.2 MHz
$p_{2,2}$	25.6 kHz	87.8 MHz
Design constrains	Dedicated NMOS pass transistor and charge pump are needed.	Offchip cap and high bandwidth of error amplifier are needed.
Reference	[30, 47, 88]	[27]

The red font shows the absolute critical parameters, while the blue font and the black font represent less critical and relax parameters, respectively.

$A_{2,DC}$ with 20 dB can not reach DC PSR of −50 dB alone, so $PSR_{2,DC}$ is used to further reduce the DC PSR according to the equation (2.14).

$$\left|\frac{PSR_{out2,DC}}{A_{out2,DC}} - PSR_{2,DC}\right| \leq PSR_{ldo,DC}A_{2,DC}A_{FB}, \tag{2.62}$$

$$\leq 3.16\times10^{-2}, \tag{2.63}$$

$$PSR_{2,DC} \in [1.02, 1.08]. \tag{2.64}$$

The value of $PSR_{2,DC}$ should be approximately 1, so that the same amount of interference on the gate and the source of the PMOS pass transistor can cancel each other out. Many state-of-the-art designs utilize this strategy, namely the

"feed-forward ripple cancellation technique". In this case, $PSR_{2,DC}$ with 1.04 (0.34 dB) was chosen.

Full-spectrum PSR

Table 2.4 shows two variants to achieve full-spectrum −50 dB PSR.

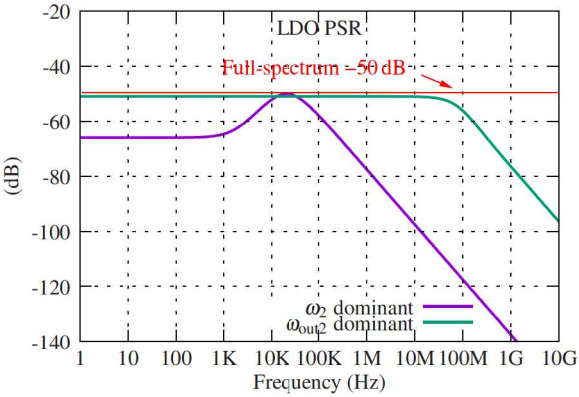


Fig. 2.15 With the parameters of Table 2.4, the simulation results show achieved full-spectrum PSR −50 dB.

If ω_2 is dominant, according the equation (2.29), the peak PSR decreases as $PSR_{\text{out2,DC}}$ decreases. $PSR_{\text{out2,DC}}$ can be set directly to −50 dB, while $A_{2,\text{DC}}$ is set slightly higher than 50 dB and the other parameters are totally relax. To achieve a $PSR_{\text{out2,DC}}$ of −50 dB without affecting $A_{\text{out2,DC}}$, the PMOS pass transistor is not sufficient. A NMOS pass transistor and a charge pump [46] can be utilized, since $g_{\text{ds,N}}$ is naturally much smaller than $g_{\text{m,N}}$.

If ω_{out2} is dominant, the off-chip capacitor should be also needed to pull f_{out2} to a low frequency. $A_{2,\text{DC}}$ needs to be at least 50 dB to achieve a DC PSR of −50 dB. Therefore, f_2 needs to be pushed to a high frequency, which is 191 MHz in this case.

2.4 Time-domain temperature sensor topology

2.4.1 Overview of voltage-domain temperature sensors

In order to achieve a low-power time-domain temperature sensing, the state-of-the-art voltage-domain concepts [31, 37, 5, 51] have to be studied. While many characteristics in CMOS are temperature dependent, the characteristic utilized to generate a voltage signal can be designed to generate a time signal as well. In CMOS the bipolar transistors are widely adopted to generate a proportional-to-absolute-temperature (PTAT) voltage and a temperature independent bandgap reference voltage.

In Fig. 2.16 the diode-connected PNP transistors Q1 and Q2 are used to generate the base-emitter voltages V_{BE1} and V_{BE2}. The voltage difference ΔV_{BE} between V_{BE1} and V_{BE2} is amplified by the factor α and produces the PTAT voltage $\alpha\Delta V_{BE}$. The sum of V_{BE1} and $\alpha\Delta V_{BE}$ is obtained as the reference bandgap voltage V_{REF}. The analog-to-digital converter (ADC) converts the voltage $\alpha\Delta V_{BE}$ and produces the digital temperature code D_{out}.

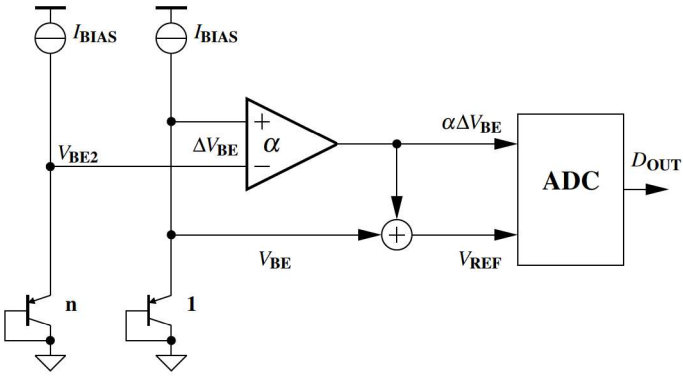


Fig. 2.16 Operational principle of the voltage-domain temperature sensor [31]

The base-emitter voltage of a bipolar transistor in the forward-active region can be written as:

$$V_{\mathrm{BE}} = \frac{kT}{q} \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right), \tag{2.65}$$

where k denotes Boltzmann's constant, q the elementary charge, and T absolute temperature in Kelvin, I_{S} the transistor's saturation current and the I_{C} the collector's current.

The transistor's saturation current can be written as [2]:

$$I_{\mathrm{S}} = bT^{4+m} e^{\frac{-E_g}{kT}}, \tag{2.66}$$

where b is a proportional factor, $m \approx -3/2$ and $E_g \approx -1.2\,\mathrm{eV}$.

The collector's current I_{C} is held constant over temperature. Thus, the temperature coefficient of V_{BE} can be written as:

$$\frac{\partial V_{\mathrm{BE}}}{\partial T} = \frac{k}{q} \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right) - \frac{kT}{qI_{\mathrm{S}}} \frac{\partial I_{\mathrm{S}}}{\partial T}. \tag{2.67}$$

Finally, the coefficient of equation 2.67 can be expressed by [2]:

$$\frac{\partial V_{\mathrm{BE}}}{\partial T} = \frac{V_{\mathrm{BE}} - (4+m)V_T - E_g/q}{T}. \tag{2.68}$$

Equation 2.68 shows that the temperature coefficient of V_{BE} is dependent on the magnitude of V_{BE} itself. The value of $\partial V_{\mathrm{BE}}/\partial T$ is technology dependent.

If two bipolar transistors are biased with different currents, the difference of base-emitter voltages can be expressed by:

$$\Delta V_{\mathrm{BE}} = V_{\mathrm{BE}} - V_{\mathrm{BE2}} = \frac{kT}{q} \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{C}}/n}\right) = \frac{kT}{q} \ln(n), \tag{2.69}$$

where n is the ratio between two bipolar transistors (Fig. 2.16). The temperature coefficient can be easily expressed by:

$$\frac{\partial \Delta V_{\mathrm{BE}}}{\partial T} = \frac{k}{q} \ln(n). \tag{2.70}$$

Obviously the temperature coefficient is PTAT.

A bandgap reference voltage can be built based on V_{BE} and ΔV_{BE}. The reference voltage is obtained by adding an amplified voltage of ΔV_{BE} to V_{BE} and results in a temperature-independent voltage V_{REF}:

$$V_{\mathrm{REF}} = V_{\mathrm{BE}} + \alpha \cdot \Delta V_{\mathrm{BE}}, \tag{2.71}$$

where α is the amplification gain of ΔV_{BE}.

An ADC, which converts the ratio of $\alpha \Delta V_{\mathrm{BE}}$ to V_{REF}, is utilized to obtain the digital code D_{OUT} [31]:

$$D_{\mathrm{OUT}} = A \cdot \frac{\alpha \Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}} - B. \tag{2.72}$$

In a typical CMOS technology, for example, V_{BE} can be simulated with 630 mV at $T = 300$ K. The value of $\partial V_{\mathrm{BE}}/\partial T$ can be calculated with approximately $-2.12\,\mathrm{mV/K}$. With the temperature from –40 °C (233 K) to 125 °C (398 K) the voltage V_{BE} and its temperature coefficient vary from 770 mV to 420 mV and from –2.06 mV/K to –2.18 mV/K (Fig. 2.17), respectively. The average temperature coefficient is –2.12 mV/K.

To build up the bandgap voltage, the ratio n can be selected with any integer between 2 and infinity. However, with the consideration of using chip area efficiently, the ratio with a range of 2 to 48 is recommended. For example, with the n of 8, the PTAT temperature coefficient results in approximately 0.179 mV/K. In this example, the gain α is calculated as 11.84. With this gain, the V_{REF} generates approximately 1.25 V in Fig. 2.16.

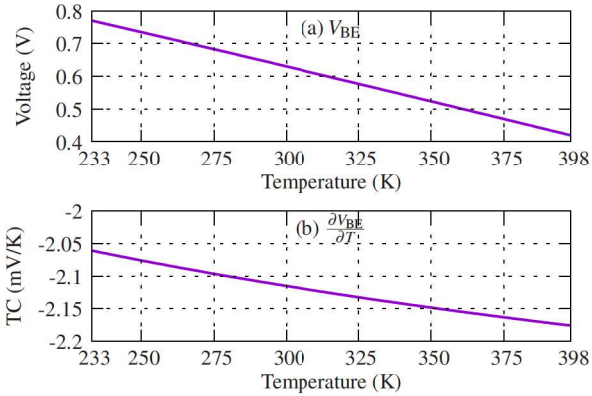


Fig. 2.17 (a) Temperature dependency of the base-emitter voltage V_{BE} and (b) its temperature coefficient in a typical CMOS technology

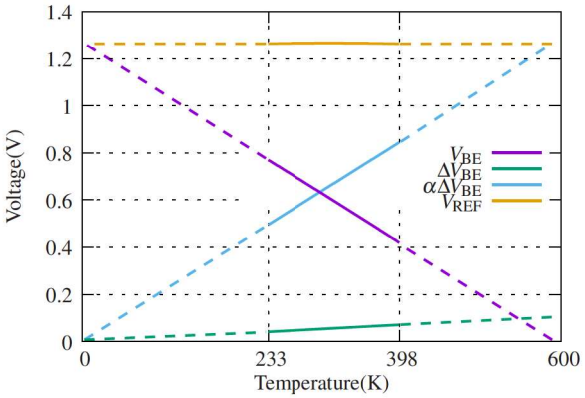


Fig. 2.18 Temperature dependency of the voltages in Fig. 2.16

2.4.2 Conversion of voltage-domain to time-domain

In order to perform the conversion from voltage-domain to time-domain in regular order, Fig. 2.16 and Fig. 2.18 need to be considered. In Fig. 2.19 the voltages

of Fig. 2.16 such as V_{BE}, ΔV_{BE}, $\alpha\Delta V_{BE}$ and V_{REF} are converted into the corresponding timing signals t_{VBE}, $t_{\Delta VBE}$, $\alpha t_{\Delta VBE}$ and t_{REF}, respectively. The timing signals are evaluated in a time-to-digital converter (TDC) instead of an ADC. The same D_{OUT} should be obtained from both voltage-domain and time-domain systems.

In Fig. 2.20 the timing signals are plotted for temperature dependence, which should be similar to Fig. 2.18.

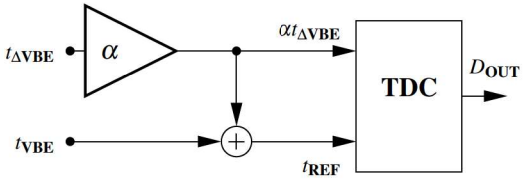


Fig. 2.19 Consideration of converting voltage signals in Fig. 2.16 into timing signals

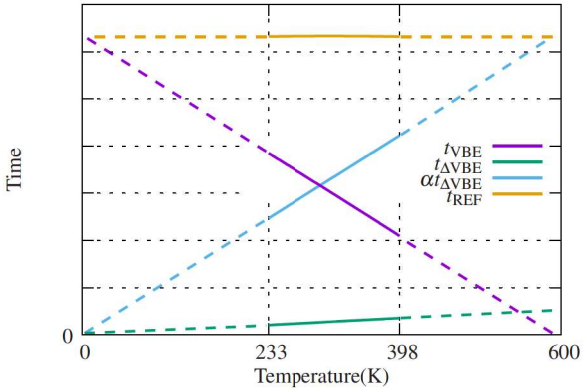


Fig. 2.20 Temperature dependence of the timing signals in Fig. 2.19

Fig. 2.21 [85] shows the block diagram of the proposed temperature sensor, which consists of a delay generator and a TDC. The delay generator generates

a PMW signal, which includes the information of $\alpha t_{\Delta VBE}$ and t_{REF} in Fig. 2.19. The TDC measures the duty cycle of the PWM signal, which can be expressed by:

$$Duty = \frac{\alpha t_{\Delta VBE}}{t_{REF}}. \tag{2.73}$$

The TDC outputs a corresponding digital code D_{out} at the end of each conversion cycle, which is indicated by asserting the *Done* signal.

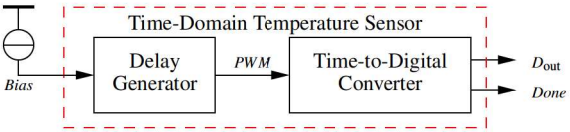


Fig. 2.21 Block diagram of the proposed time-domain temperature sensor [85]

2.4.3 Sensor modeling

Switched-capacitor (SC) circuits can be used to generate the timing signals. In Fig. 2.22 (a), the current I flows through the capacitor C, when the switch S_1 turns off. The comparator evaluates the capacitor voltage V_{IN} continuously and inverts the output voltage V_{OUT}, when V_{IN} reaches the reference voltage V_{REF}. The charging time t can be written by:

$$t = \frac{C}{I} \cdot V_{REF}. \tag{2.74}$$

It is easy to see that the t is proportional to V_{REF}. By manipulating I and C, the resulting time can obtain within any desired range.

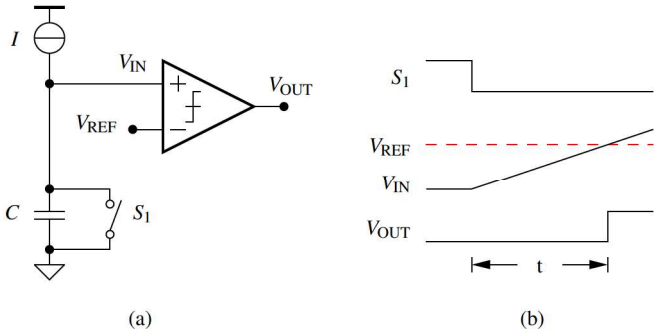


Fig. 2.22 (a) Switched-capacitor circuit is suitable to generate (b) timing signal t , which is proportional to V_{REF}.

Timing generation for negative TC

The timing with negative TC t_{VBE} can be generated by the circuit model in Fig. 2.23. The time can be expressed by:

$$t_{\mathrm{VBE}} = \frac{C_1}{I} \cdot V_{\mathrm{BE}} \tag{2.75}$$

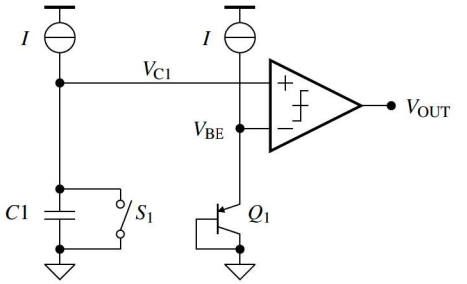


Fig. 2.23 SC circuit combined with V_{BE} generates a timing signal with negative temperature coefficient

Timing generation for positive TC

Fig. 2.24 shows the timing $t_{\Delta VBE}$ Generation. The capacitor C_2 is located above the bipolar transistor Q_2, which is n times larger than Q_1. Due to the fact that Q_1 and Q_2 are biased by same current I, current density of Q_2 is n times less than Q_1.

$$t_{\Delta VBE} = \frac{C_2}{I} \cdot \Delta V_{BE} \tag{2.76}$$

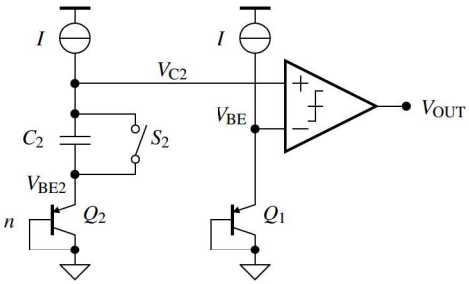


Fig. 2.24 SC circuit combined with two V_{BE} voltages generates a timing with positive temperature coefficient

Timing generation for zero TC

In order to generate the timing signal t_{REF}, which is the sum of t_{VBE} and $\alpha t_{\Delta VBE}$, two consecutive timing signals have to be triggered. A control logic can be used to control S_1 and S_2. Only one comparator is utilized to save energy and chip area. Fig. 2.25 [87] shows the model of the delay generator. The structure contains three analog paths, which are supplied with copies of the bias current I_{BIAS}. The right-most path consists of C_1 and S_1. Opening or closing S_1 causes C_1 to be charged by I_{BIAS} or discharged, respectively. The central path is formed by the diode-connected bipolar transistor Q_1, which generates the voltage V_{BE}. The left-most path consists of C_2, S_2 and Q_2. S_2 is used to reset C_2. Q_2 has n

times the emitter area of Q_1 and generates the voltage V_{BE2}. Depending on the position of S_3, the comparator compares V_{C1} or V_{C2} with V_{BE}.

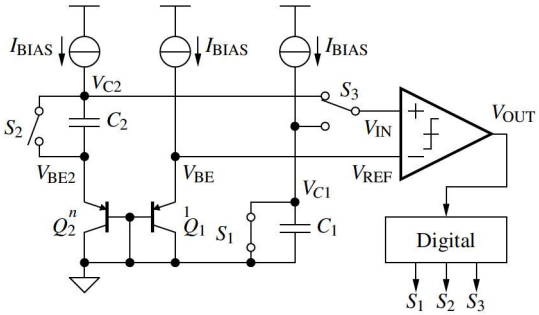


Fig. 2.25 The complete model combines two structures from Fig. 2.23 and Fig. 2.24.

The timing signals t_{VBE} and $\alpha t_{\Delta VBE}$ are given by:

$$t_{VBE} = \frac{C_1 \cdot V_{BE}}{I_{BIAS}}, \tag{2.77}$$

$$\alpha t_{\Delta VBE} = \frac{C_2 \cdot (V_{BE} - V_{BE2})}{I_{BIAS}} = \frac{C_2 \cdot \Delta V_{BE}}{I_{BIAS}}. \tag{2.78}$$

The PWM period t_{REF} is given by the total charging time:

$$t_{REF} = t_{VBE} + \alpha t_{\Delta VBE} = \frac{C_1 V_{BE} + C_2 \Delta V_{BE}}{I_{BIAS}}. \tag{2.79}$$

The corresponding duty cycle D can be expressed as:

$$Duty = \frac{\alpha t_{\Delta VBE}}{t_{REF}} = \frac{C_2 \Delta V_{BE}}{C_1 V_{BE} + C_2 \Delta V_{BE}}. \tag{2.80}$$

Let TC_{VBE} and $TC_{\Delta VBE}$ denote the temperature coefficients of V_{BE} and ΔV_{BE}, respectively. If the capacitance ratio $\alpha = C_2/C_1$ is chosen such that

$\alpha = |TC_{VBE}/TC_{\Delta VBE}|$, then

$$Duty = \frac{C_2 \Delta V_{BE}}{C_1(V_{BE} + \alpha \Delta V_{BE})} = \frac{\alpha \Delta V_{BE}}{V_{REF}} = \frac{\alpha \cdot \ln(n) \cdot kT/q}{V_{REF}} = \frac{\alpha k \ln(n)}{q V_{REF}} \cdot T. \tag{2.81}$$

V_{REF} represents a virtual (calculated) bandgap voltage, which is not constructed explicitly with circuit components because it is not needed as a physical quantity. It follows from Equation 2.81 that $Duty(T)$ is proportional to absolute temperature.

The voltage-domain Equation 2.72 can be rewritten in the time-domain version:

$$D_{OUT} = A \cdot \frac{\alpha \Delta V_{BE}}{V_{REF}} - B = A \cdot Duty - B. \tag{2.82}$$

2.4.4 Parameter selection and model verification

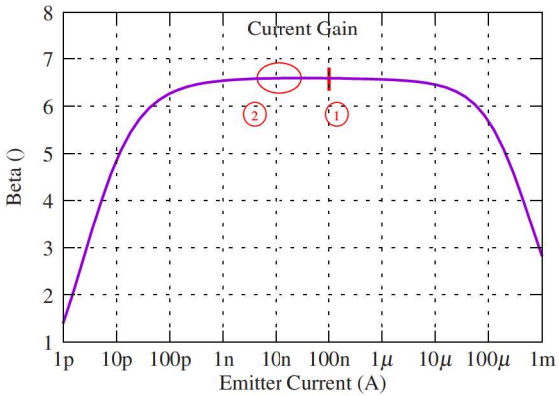


Fig. 2.26 The current gain is stable and high from 1 nA to 1 µA. By choosing I_{BIAS} of 100 nA, the current density of Q_1 and Q_2 (Fig. 2.25) can be obtained at ① and ②, respectively.

Although I_{BIAS} is not shown in the equation 2.81, it is still related to some crucial parameters, such as the matching between Q_1 and Q_2 in Fig. 2.25, the

possible range of α and n in the equation 2.81 and the potential input range of the comparator in Fig. 2.25. To obtain the best possible matching between Q_1 and Q_2, not only the layout must be carefully designed, but also the current gain (beta) of the bipolar transistor needs to be chosen with the highest possible value. The simulation result of beta versus its emitter current of a typical bipolar transistor in a commercial CMOS technology [84] is shown in Fig. 2.26. With the emitter current range of 1 nA to 1 µA, the beta is relatively high and stable with a value of 6.6. To achieve a low-power design, the emitter current should be as low as possible. However, since the current density of Q_2 in Fig. 2.25 is reduced by the factor of n, the emitter current of Q_2 should be still in the stable range. In this design, I_{BIAS} is chosen with 100 nA (Fig. 2.26 ①), so that Q_2 also gets an appropriate current density with different n (Fig. 2.26 ②).

Table 2.5 Parameters of the components in model

Component	Parameter
C_1	60 pF
C_2	678 pF
n	8
α	11.3
I_{BIAS}	100 nA

The parameters n and α are set together. In the equation 2.81 the choice of a large n will not bring big benefit compared to a large α for a better sensitivity of the duty cycle. In this design, n is chosen with 8 so that the total number of bipolar transistors Q_1 and Q_2 is 9. It is convenient to create the layout with a 3X3 array with common centroid. With $n = 8$, α can be calculated with 11.3 to generated the temperature independent time t_{REF}.

The choice of C_1 and C_2 in equation 2.80 is constrained by the bandwidth of the sensor. In equation 2.79, the period of the sensor t_{REF} defines the sampling rate. The larger the capacitors, the longer the sensor runs, resulting in a small sensor bandwidth. Large capacitors occupy large chip area as well. On the other

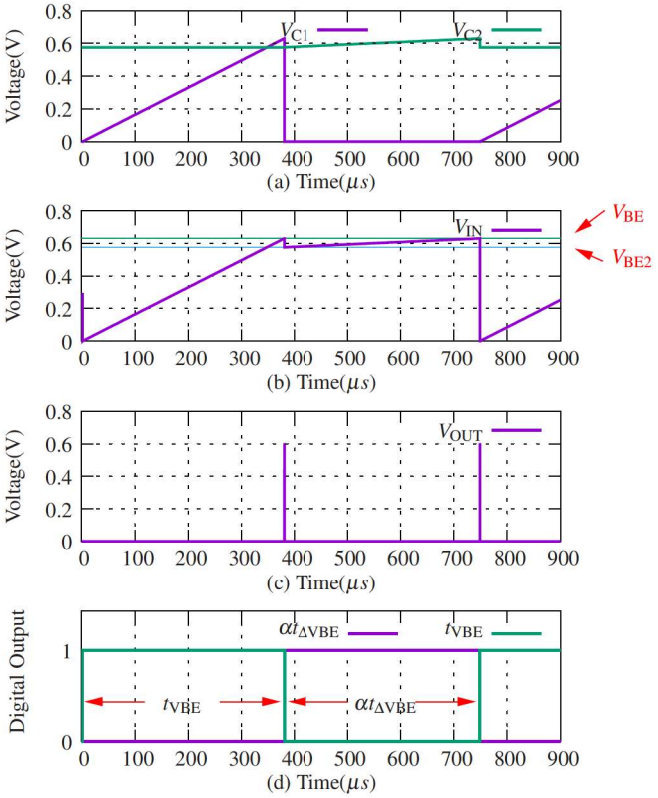


Fig. 2.27 Transient simulation results of the analog voltages and the digital controls

hand, the small cap size leads to a high bandwidth and area efficient design, while the requirement of TDC is dramatically increased, because TDC requires a higher clock frequency to extract the time. In this design, the period is set to approximately 1 ms, so the TDC runs easily with MHz clock. C_1 and C_2 are set by 60 pF and 678 pF, respectively. The parameters are summarized in Table 2.5.

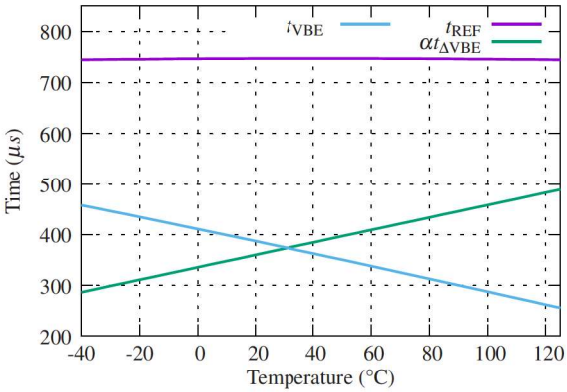


Fig. 2.28 Temperature dependence of t_{REF}, $\alpha t_{\Delta VBE}$ and t_{VBE}

The transient simulation is carried out at room temperature. In Fig. 2.27 (d) the period from 1 µs to 747 µs is divided into two pulses: t_{VBE} and $\alpha t_{\Delta VBE}$. In Fig. 2.27 (a) during t_{VBE} the voltage V_{C1} rises from 0 V to 630.4 mV, while the voltage V_{C2} rises from 576.1 mV to 630.4 mV during $\alpha t_{\Delta VBE}$. The input voltage V_{IN} of the comparator is switched between V_{C1} and V_{C2} in Fig. 2.27 (b) and compared with V_{BE}. The output voltage V_{OUT} of the comparator can be observed with two spikes in Fig. 2.27 (c). The sensor runs continuously without external controls.

This transient simulation is performed from –40 °C to 125 °C. In Fig. 2.28 it can be seen that the timing signal t_{REF} remains at 745 µs, while $\alpha t_{\Delta VBE}$ increases linearly from 286 µs to 489 µs in the whole temperature range.

The duty cycle in Fig. 2.29 shows that from –40 °C to 125 °C the duty cycle increases linearly from approximately 38.5 % to 65.7 %.

The conversion of the duty cycle to the temperature is carried out with the help of:

$$T_{OUT} = 606.4 \cdot Duty - 273. \tag{2.83}$$

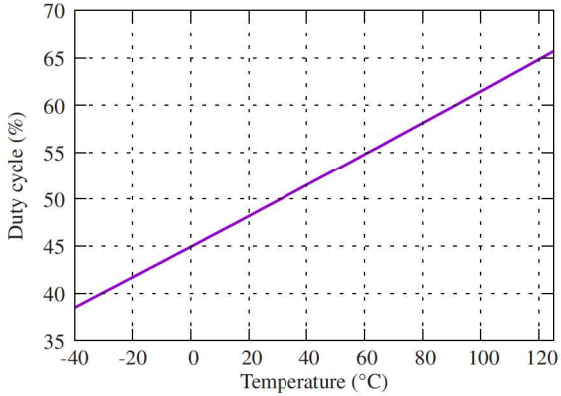


Fig. 2.29 Temperature dependence of the duty cycle

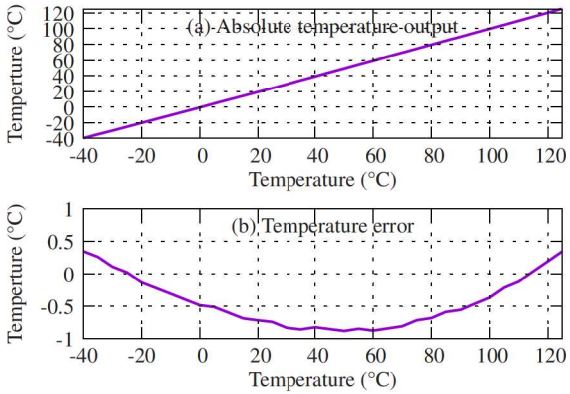


Fig. 2.30 Temperature accuracy with (a) absolute temperature output and (b) its error

The temperature output shows a relatively good linearity in Fig. 2.30 (a) from –40 °C to 125 °C. The temperature error in Fig. 2.30 (b) is obtained from –0.85 °C to 0.34 °C. The error is not proportional to the input temperature due to the second-order effect (curvature effect).

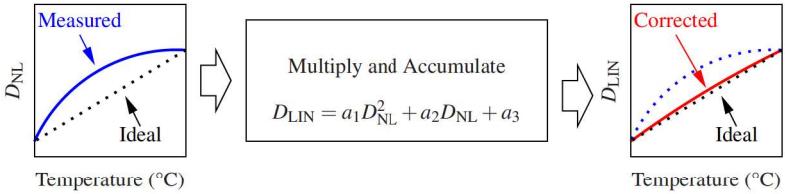


Fig. 2.31 Systematic non-linearity correction concept [7]

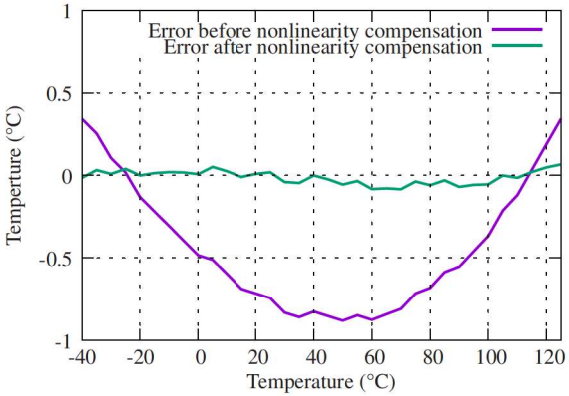


Fig. 2.32 Temperature accuracy is improved by a factor of 8 after applying non-linearity compensation

To overcome this non-linearity error, the result must be corrected by second-order polynomial. The concept [7] in Fig. 2.31 can be used to remove the non-linearity. The polynomial correction block is a second-order multiply-and-accumulate unit. The input is the nonlinear duty cycle, while the output is linearized duty cycle. This method can be utilized to remove the systematic non-linearity, but not suitable for process mismatches. After the non-linearity compensation the temperature error is reduced to $[-0.08, 0.06]$ °C in Fig. 2.32. Comparing the results without non-linearity compensation, the temperature sensing

accuracy is improved by a factor of 8. The residual error is caused by the higher order non-linearity and the inaccuracy of the simulator.

2.5 Digitization of the supply noise and comparison

To systematic analyze the sensor performance under supply noise, it makes sense to compare the performance with other state-of-the-art designs.

2.5.1 Modeling of the state-of-the-art sensor topologies

Common structure

Fig. 2.33 (a) shows the proposed common structure of the time-domain temperature sensor. The delay generator consists of one or more delay cells, which are separated in one or more paths. The TDC measures the delay between the delay input and output and generates a digital code. The delay cell (Fig. 2.33 (b)) consists of an analog delay and a digital propagation delay. For the analog delay, SC circuits are usually used to charge/discharge capacitors. Such SC circuits need a "start" signal to initiate. In Fig. 2.33 (c) two SC circuits generate slope signals S_1 and S_2, which are connected to the input of a comparator. The SC delay is generated until S_1 and S_2 cross. The comparator output signal S_3, which is a digital signal, is shown in Fig. 2.33 (c). Digital logic gates that can be added to the model, also cause a propagation delay. All propagation delays together can be combined into a digital delay block, that indicates the delay from the cross time of S_1,S_2 to the rising edge of S_4.

The whole delay cell is basically the temperature sensing block, since all the components can be sensitive to temperature. Since the components are connected to the supply voltage, their supply sensitivity should be also considered. TDC is basically a digital block controlled by the system clock. The system clock can be extracted by the RFID carrier frequency, which is independent of

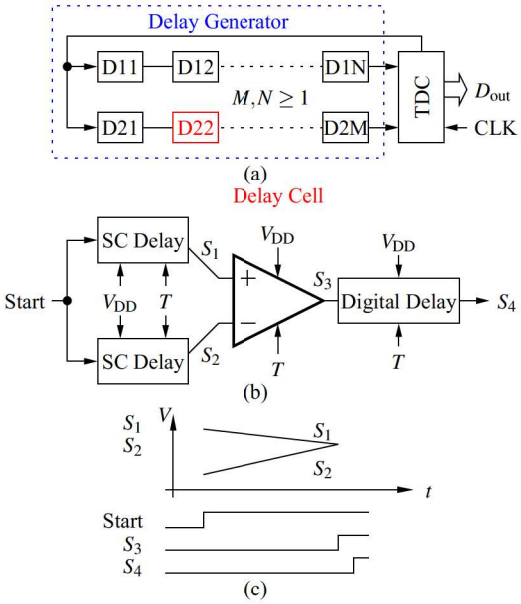


Fig. 2.33 The proposed the common structure (a), which can be used to analyze the common time-domain temperature sensor topologies. The common structure of the single delay cell (b) and the diagram of the internal signals

temperature and supply voltage. Therefore, the TDC is considered as an ideal block in this paper.

In the models, every block of Fig. 2.33 (b) is modeled via VerilogA. The supply and temperature are given to the blocks as input parameters. The VerilogA model is coded on the basis of physical equations representing the operation principle of transistor circuits.

Inverter based topology

Inverter based topology has been widely used in time-domain temperature sensors [12, 7, 20]. Inverters can be considered as comparators that compare the in-

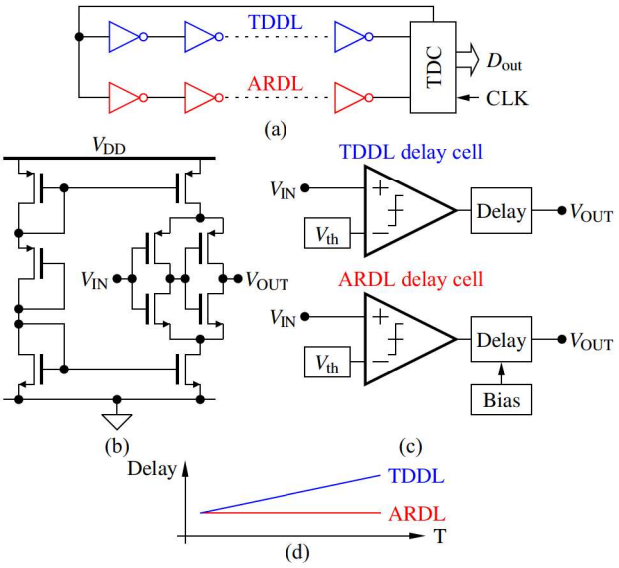


Fig. 2.34 (a) Topology of [12], (b) Circuit of a ARDL delay cell, (c) Models of TDDL nad ARDL delay cell, (d) Delay of TDDL and ARDL vs. temperature

put voltage and their own switching threshold, while the output signal is shifted by a propagation delay. In Fig. 2.34 (a) [12] the inverters form two different delay paths, which are temperature dependent delay line (TDDL) and adjustable reference delay line (ARDL), respectively. TDDL consists of the conventional inverter, whose model is shown in Fig. 2.34 (c). The voltage V_{th} is the threshold voltage of the inverter with the value, which is normally half of the supply voltage V_{DD}. ARDL consists of a customized delay cell (Fig. 2.34 (b)), which is biased by a dedicated current, so that the delay is independent of the temperature. The model of ARDL (Fig. 2.34 (c)) shows that the propagation delay is turned by the bias current. In Fig. 2.34 (d) the cell TDDL has a PTAT delay while the delay of ARDL is temperature independent. By configuring the multiplier of ARDL to match TDDL, the temperature can be determined.

In the modeling, the propagation delay is expressed by

$$t_{\text{delay}} \propto \frac{C_{\text{L}} \cdot V_{\text{DD}}}{\mu C_{\text{OX}} \frac{W}{L} (V_{\text{DD}} - V_{\text{th}})^2}, \tag{2.84}$$

where μ is the mobility of electrons/holes, C_{OX} is the gate-oxide capacitance per unit area, W and L are the width and length of the MOS transistors, V_{DD} is the supply voltage, V_{th} is the threshold voltage (assuming that NMOS and PMOS have the same threshold voltage), and C_{L} is the load capacitance of the inverter stage. In the equations the mobility and threshold voltage are temperature dependent. The dependency can be written as

$$\mu \propto \mu_0 (T/T_0)^{-p}, \tag{2.85}$$

$$V_{\text{th}} = V_{\text{th0}} - m(T - T_0). \tag{2.86}$$

where p is a parameter typically in the range of 1.2 to 2, μ_0 is the mobility at room temperature T_0, V_{th0} is the threshold voltage at room temperature, and m is approximately in the range of 1 to 3 mV/°C.

It is clear that the propagation delay is nonlinear to either the supply voltage or the temperature. In practice the delay is always linearized before conversion to temperature.

SC delay cell with complementary bias

In [23] a temperature sensor was designed for a UHF RFID sensor tag. The topology utilizes a SC circuit in a delay cell and an inverter as comparator. The structure can be seen in Fig. 2.35 (a). Firstly, a bias cell (Fig. 2.35 (b)) generates both PTAT and CTAT voltages. In Fig. 2.35 (c) the voltages are applied to OpAmps and resistors to generate PTAT and CTAT currents. The currents are applied to the SC circuit in Fig. 2.35 (d). The outputs of the SC circuits V_1 and V_2 are given to two inverters, so that the digital outputs V_3 and V_4 are generated.

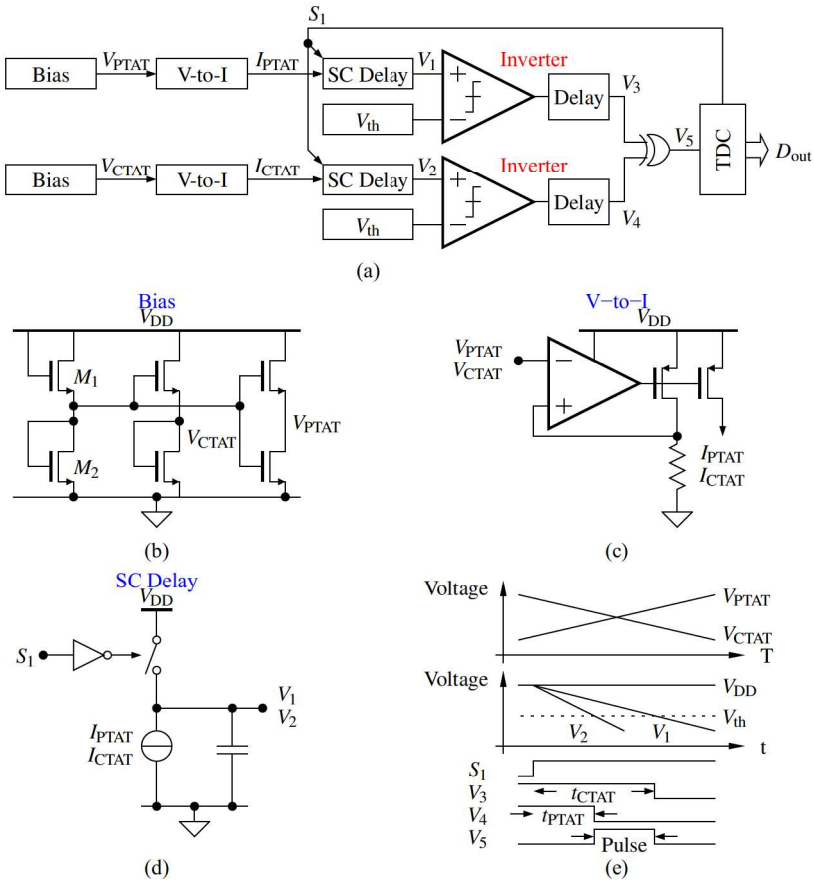


Fig. 2.35 (a) SC circuit as delay cell with two bias sources and design of (b) bias, (c) V-to-I and (d) SC circuit. (e) signals vs temperature and signals vs time

At the end, V_3 and V_4 are applied in an XOR gate. The output pulse V_5 is evaluated in TDC.

The details of the voltages on different nodes are shown in Fig. 2.35 (e). In order to generate the transient signal properly, the start signal S_1 is used. In the reset phase S_1 is open, so the switch in Fig. 2.35 (d) is closed. The supply voltage charges the capacitor to V_{DD}. Once the switch S_1 is on, the capacitor starts discharging by the currents I_{PTAT} and I_{CTAT}. The voltage drops until it reaches the switching threshold voltage V_{th} of the inverter. The output signals V_3 and V_4 are evaluated in an XOR gate to generate the final temperature dependent delay signal. As temperature increases, the PTAT current generates a shorter delay, while the CTAT current generates a longer delay. In this design, where at every temperature the CTAT delay is longer than PTAT, the pulse generated is approximately proportional to the absolute temperature.

In the modeling the I_{PTAT} and I_{CTAT} inFig. 2.35 (c) can be written as [23]:

$$I_{PTAT}(T) = I_{PTAT}(T_0)(1 + k_P(T - T_0)), \tag{2.87}$$

$$I_{CTAT}(T) = I_{CTAT}(T_0)(1 - k_C(T - T_0)), \tag{2.88}$$

where k_P and k_C are corresponding proportional constant. The PTAT and CTAT delays are generated by CTAT and PTAT currents in the SC circuit, respectively. The pulse width in Fig. 2.35 (e) can be written [23]

$$\begin{aligned} t_{Pulse}(T) \approx & \left(\frac{C\Delta V}{I_{CTAT}(T_0)} - \frac{C\Delta V}{I_{PTAT}(T_0)}\right) \\ & + \left(\frac{C\Delta V k_C}{I_{CTAT}(T_0)} - \frac{C\Delta V k_P}{I_{PTAT}(T_0)}\right)(T - T_0). \end{aligned} \tag{2.89}$$

It can be seen that the pulse width is approximately proportional to the temperature. the temperature can be obtained by reading the pulse width. The supply voltage has a large influence on I_{CTAT} and I_{PTAT}, because in Fig. 2.35 (b) M_1 and M_2 divide the supply voltage for the generation of V_{CTAT} and V_{PTAT}. Furthermore, in the SC delay block the capacitor is directly tied to the supply in the reset phase, so that any supply variation can cause different initial voltages in the discharging phase. The inverter is also sensitive to the supply voltage, since

the switching threshold voltage and the propagation delay are dependent on the supply.

SC delay cell with single bias

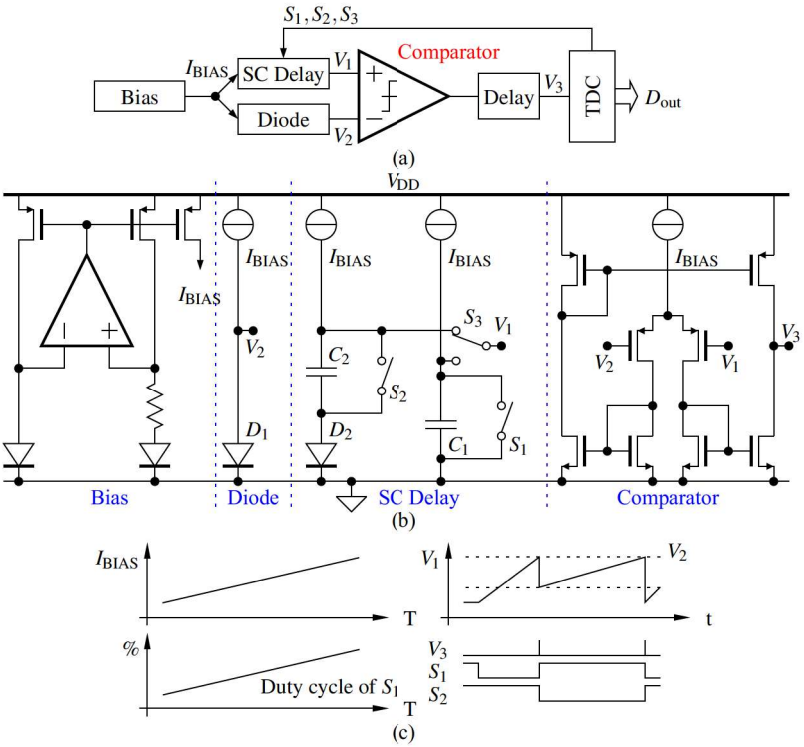


Fig. 2.36 (a) SC circuit as delay cell with single bias and design of (b) bias, reference block, SC circuit and comparator. (c) signals vs temperature and signals vs time

In the section 2.4, a SC delay cell topology with only one bias current is proposed. The simplified structure is shown in Fig. 2.36 (a). The bias block

(Fig. 2.36 (b)) generates a bias current that is delivered to the SC delay cell and reference generation. The bias current is generated in a conventional way that includes a regulation and several passive elements. In the reference generation block the bias current flows directly to a diode and generates the reference voltage V_2. The voltage V_2 is CTAT voltage over temperature. In the SC block the bias current is provided on two signal paths. In the reset phase, the capacitors C_1 and C_2 are reset, while the switches S_1 and S_2 are closed. Once S_1 is open, the bias current flows through C_1. The voltage on C_1 is given to the output node as V_1, while S_3 is switched to the C_1 path. The output voltage V_1 continues to rise until it reaches the reference voltage V_2 in Fig. 2.36 (c). Then the switches S_2 and S_1 are opened and closed, respectively. The capacitor C_2 starts charging. This time S_3 is set so that the output voltage V_1 is connected to the C_2 path. The voltage on V_1 increases from the base-emitter voltage of D_2 to the reference voltage V_2 (Fig. 2.36 (c)).

According to the previous analysis, the duty cycle of this temperature sensor can be written as 2.81:

$$Duty = \frac{C_2 \Delta V_{\mathrm{BE}}}{C_1 (V_{\mathrm{BE}} + \alpha \Delta V_{\mathrm{BE}})} = \frac{\alpha \Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}} = \frac{\alpha \cdot \ln(n) \cdot kT/q}{V_{\mathrm{REF}}} = \frac{\alpha k \ln(n)}{q V_{\mathrm{REF}}} \cdot T.$$

It follows that *Duty* is proportional to the absolute temperature (Fig. 2.36 (c)). In comparison with [23] this structure utilizes duty cycle measurement instead of pulse width measurement. On the other hand, this structure uses no inverter but a low-power conventional comparator. The effect of the supply ripple can be seen in the bias block with several current mirrors. The change of the bias current leads to the change of the reference voltage V_2 and the delay generation of the SC block. The supply voltage can also change the propagation delay of the comparator.

2.5.2 Time-domain temperature sensor topology analysis

In the publications, the sensors are realized in different technologies. In order to compare the performance fairly, it makes sense to test them in the same environment. Despite the simulations performed for models, their parameters should be adapted to the real transistors. In this analysis, all models are built via Verilog-A [55] corresponding to a transistor-level circuit in a commercial 0.18 µm technology. Since other unideal effects e.g. process variation, noise, matching go beyond the scope of this analysis, only the supply voltage is considered in the models. The three models are configured in same order for the nominal supply voltage and the temperature sensing range. All sensor data are linearized and one-point trimmed at room temperature. Suppose the sensing error is specified for ±1 °C in the temperature range of 0 °C to 100 °C with the supply variation of ±0.1 V. The DC supply sensitivity is defined in the following equation:

$$DC\ Sensitivity = \frac{Maximum\ error\ amplitude}{Supply\ variation}, \tag{2.90}$$

$$= \frac{Error_{\max} - Error_{\min}}{Supply\ variation}. \tag{2.91}$$

Thus, the DC sensitivity is specified for 0.01 °C/mV.

An example of DC sensing error of SC delay cell with complementary bias is shown in Fig. 2.37. All of the curves cross at room temperature, since they are trimmed by room temperature. It can be seen that at nominal supply voltage (1.8 V) this temperature sensor reaches the specification. When the supply voltage increases or decreases, the curve slopes with various gradients. For inverter based topology and the SC delay cell with complementary bias, errors vary in the range of −3.5 °C to 2.7 °C and −2.7 °C to 3.3 °C, respectively. The topology with single bias only generates <0.1 °C error.

The sensitivity of all three sensors are summarized in Table 2.6.

The results clearly show that the topology with single bias, which is proposed by this dissertation, achieves the most robust DC supply sensitivity. How-

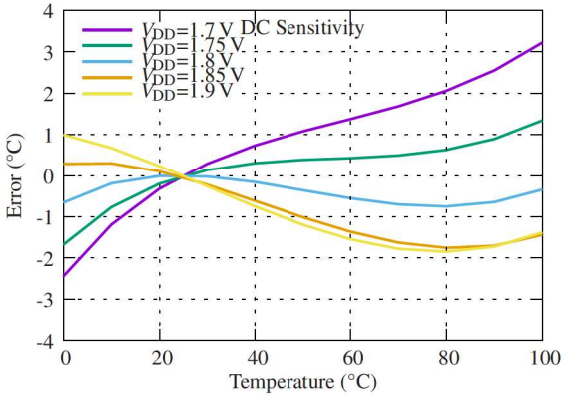


Fig. 2.37 The DC sensitivity of the topology: SC delay cell with complementary bias

Table 2.6 Performance summary of supply sensitivity with the specification of 0.01 °C/mV

Topology	Supply Sensitivity	Pass/Fail
Inverter based topology	0.031 °C/mV	Fail
SC delay cell with complementary bias	0.03 °C/mV	Fail
SC delay cell with single bias	0.0006 °C/mV	Pass

ever, since the noise is distributed in a wide frequency spectrum, the AC supply sensitivity needs to be investigated. In the analysis of the AC supply sensitivity, a sinusoidal voltage is added to DC supply voltage in the frequency range from 10 Hz to 1 MHz. The topology *SC delay cell with single bias* is only followed and adopt to the analysis.

The data process flow can be seen in Fig. 2.38, which utilizes 10 Hz AC signal with 100 mV amplitude as stimulus signal at room temperature (27 °C). In 100 ms, V_{DD} swings between 1.9 V and 1.7 V. Since the temperature sensor

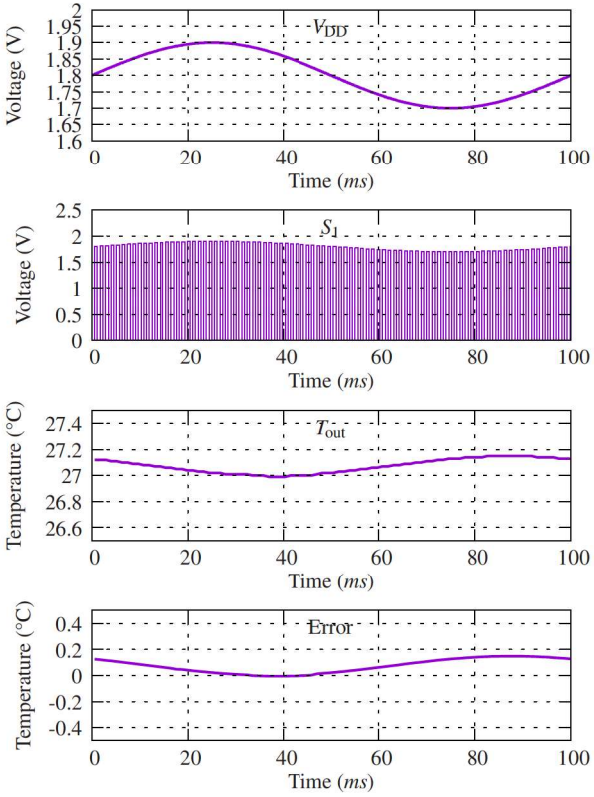


Fig. 2.38 The internal signals of an AC sensitivity simulation with 10 Hz stimulus AC signal.

has approximately 1 ms conversion time, it generates a large number of pulses during this time. By evaluating each pulse the duty cycle and further the output temperature can be determined. In Fig. 2.38 the output temperature is generated in the range of approximately 27 °C to 27.14 °C, which corresponds to the error within 0 °C to 0.14 °C. Finally, the error is calculated over time so that the

maximum error can be taken into account as final error for that frequency. In this case 0.14 °C is the final error at this frequency of 10 Hz.

The temperature sensor model is tested in a wide spectrum up to 1 MHz, which includes RFID communication and sensor sampling frequency. The injected AC stimulus signal features a 200 mV $V_{p\text{-}p}$ amplitude, which shares the same range as the DC simulation. In this case the temperature is set at the room temperature (27 °C), whose error is trimmed in the DC sensitivity simulation. In Fig. 2.39 (a), it can be seen that the AC response is completely different from the DC response. The error, which increases and decreases with increasing frequency, can be categorized into three frequency ranges.

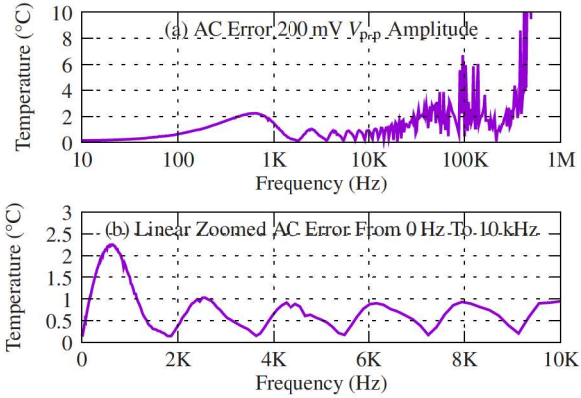


Fig. 2.39 (a) The error in the frequency domain from 10 Hz to 1 MHz and (b) its linear zoom from 0 Hz to 10 kHz

In the low frequency range from 10 Hz to 300 Hz in Fig. 2.39 (b), the error is almost linear to frequencies. This means, that the supply voltage may not reach the maximal supply rail in the phases (see S_1, S_2 and S_3 in Fig. 2.36 (c)) in one sampling period.

The error is mainly caused by the reference voltage on the comparator input, which can be simplified in Fig. 2.40 (a). The slowly changing supply voltage V_{dd} causes only slowly changing bias current I_{bias}. I_{bias} generates different volt-

age reference V_{REF} as well as different slopes of V_C. With the two combined influences, V_C reaches V_{REF} at different timings. In Fig. 2.40 (b) three different frequencies generate different reference voltages (V_{REF1}, V_{REF2} and V_{REF3}), different capacitor voltages (V_{C1}, V_{C2} and V_{C3}) and different timings (t_1, t_2 and t_3). This results in timing errors that are converted to temperature errors at the end.

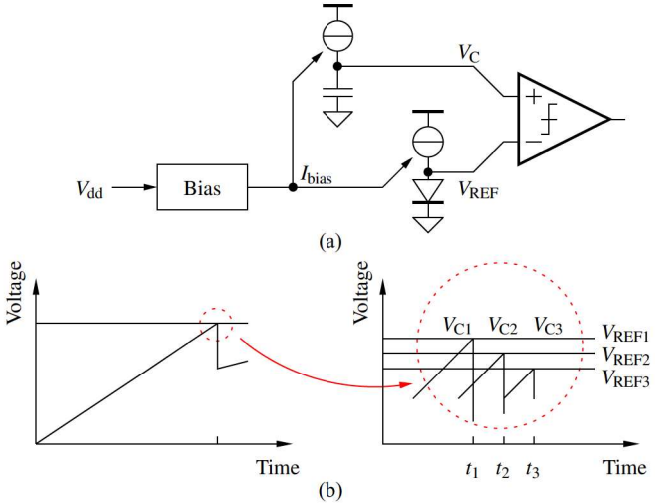


Fig. 2.40 Explanation of conversion from AC supply to time error in the very low frequency range

From 300 Hz to 10 kHz (Fig. 2.39 (b)) the supply ripple has a comparable frequency with the sensor sampling rate, which is approximately 900 Hz. In this range the error indiucates a periodic characteristic. At 630 Hz the error reaches the maximum value 2.25 °C, while the error achieves the minimum value at approximately even harmonics of its sampling frequency (1.8 kHz, 3.6 kHz, 5.4 kHz, 7.2 kHz and 9 kHz). The reason is that the phase of the PWM signal is synchronous to the supply ripple. Each phase suffers proportionally from the supply ripple, so that the duty cycle and further the sensor output are not affected by the ripple. Please notice that the maximum error does not occur at

its own sampling frequency (900 Hz) but at a lower frequency (630 Hz), due to the similar reason. The explanation can be seen in Fig. 2.41, which shows the internal simulation signals at 630 Hz. At 630 Hz, two phases of the PWM signal (Fig. 2.41 (b)) are completely mismatched, so that the duty cycle and further the sensor output (Fig. 2.41 (c)) are obtained with maximum error (Fig. 2.41 (d)).

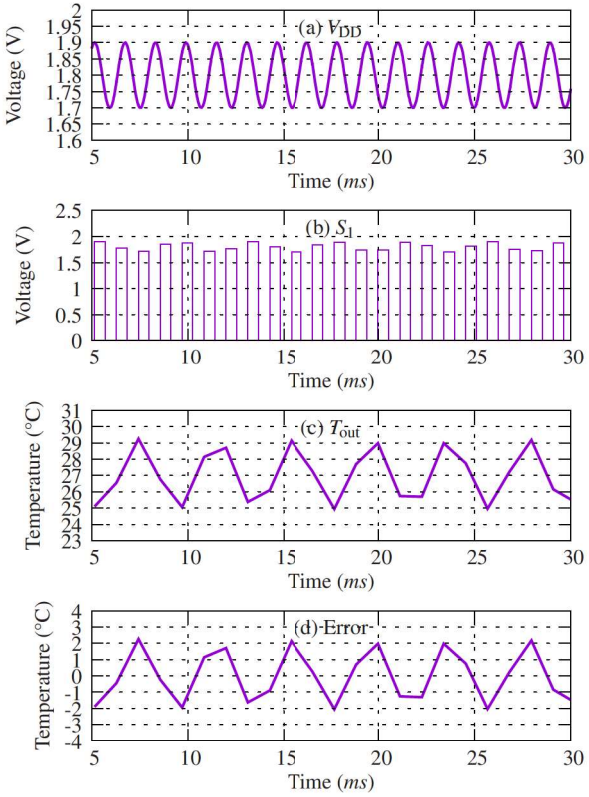


Fig. 2.41 The internal signals of an AC sensitivity simulation with 630 Hz stimulus AC signal.

Beyond 10 kHz the supply ripple can occur so often in a sampling period, that the error in Fig. 2.39 (a) becomes unpredictable . The peak error increases to 10 °C at approximately 478 kHz. Beyond 478 kHz the sensor becomes too inaccurate to be used.

In Fig. 2.42 (a), the errors are scaled logarithmically. A reached maximal error in the high frequency is drawn in the red line. It can be seen that this maximal error has approximate properties of 20 dB/Decade, which corresponds to the ripple of the bias current in high frequency in Fig. 2.42 (b). The bias current is essentially comparable to a high pass filter. The cut-off frequency of this bias current is set to 10 kHz. This indicates that beyond 10 kHz the errors are dominated by the bias current.

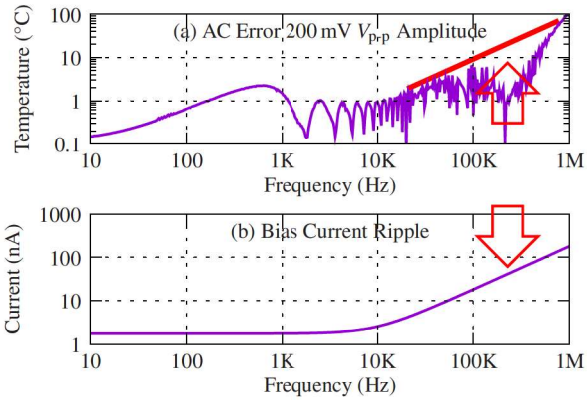


Fig. 2.42 (a) The error in the frequency domain from 10 Hz to 1 MHz and (b) the bias current ripple in the same frequency range.

2.6 Summary

This chapter introduces a novel low-power time-domain temperature sensor topology and a design methodology for analyzing supply noise.

The analysis of a voltage-domain temperature sensor shows that the theory can be utilized for a time-domain temperature sensor as well. In the time-domain temperature sensor topology, a PTAT timing signal t_{PTAT} and a CTAT timing signal t_{CTAT} are generated. With the combination of t_{PTAT} and t_{CTAT}, a temperature independent timing signal t_{REF} is generated, so that the duty cycle of t_{PTAT} ($t_{\mathrm{PTAT}}/t_{\mathrm{REF}}$) is proportional to the absolute temperature. The simulation results of the modeling show that the inaccuracy is in the range of $[-0.08, 0.06]$ °C after non-linearity compensation.

The supply noise analysis includes the generation of the noise, the amplification of the noise and the digitization of the noise. The supply noise is generated from different sources, e.g. carrier frequency, RFID communication, load condition and geometry, so that it covers a wide frequency spectrum. Then the supply noise is amplified by the PMU, which includes bandgap reference and LDO. To analyze the frequency response of the amplification (PSR), the typical models of bandgap reference and LDO are created. The PSR simulation shows that the PMU amplifies the supply interference in the RFID communication frequency band. This amplified supply noise will affect the performance of the temperature sensor. To compare the performance of this proposed temperature sensor, two other state-of-the-art time-domain temperature sensors are modeled. In DC analysis, the model of this proposed temperature sensor reaches 0.0006 °C/mV, which is lowest among the three topologies. In AC analysis, the proposed temperature sensor outputs more noise, as the frequency of the supply noise increases. This means, that the sensor will suffer significantly from the supply noise during RFID communication.

Chapter 3

Mixed-signal circuit implementation

3.1 Introduction

Although many systematic challenges in the behaviour domain are analyzed, new design challenges in the structure domain become significant. In modeling of the temperature sensor, most components are described by ideal elements, equations and programs. The behaviour of those components is linear, while all real components behave more or less nonlinear. If the non-linearity is significant enough, the performance of the sensor is affected, so that system errors could be shown in the circuit simulation results. Since the sensor topology utilizes SC circuits, the on-resistance and off-resistance of the switches must be taken into account. Due to the low-power design of the sensor, the current consumption of the comparators is extremely low so the comparators produce significant delays. Since the timing error is converted into the accuracy error in the time-domain topology, the propagation delay of the comparator is also crucial. The second challenge is the process, voltage and temperature variations

(PVT variations). The PVT variation [29] is caused by the CMOS manufacture process, which generates a small random variation on each individual transistor across the entire wafer. These variations cause the electrical parameter variations of the transistors such as threshold voltage, gate/source capacitor and cutoff frequency. In this sensor topology, the offset voltage of the comparator is caused by the PVT variation. The offset voltage introduces a timing error, so this voltage must to be minimized as well.

In this chapter, the crucial non-linearities of the circuit blocks are analyzed and optimized. The remaining non-linearities are trimmed using two-point trimming with data processing. The PVT variation is tested under Monte-Carlo simulation, so that the variation of the sensor accuracy can be determined. The temperature sensor is implemented on a test chip that is verified and measured without the RFID interface. The schematic of the top level and the layout of the test chip are presented. Finally, the experimental results and the performance comparison with other state-of-the-art time-domain temperature sensor are given. The implementation of the PMU and the frontend are explained in detail for the RFID functional blocks. The simulation results of the RFID blocks are also presented.

This chapter is organized as follows. In section II, the temperature sensor implementation is presented. The PMU and the frontend design are introduced in section III. Finally, conclusions are drawn in section IV.

3.2 Temperature sensor implementation

When implementing the time-domain topology in a CMOS circuit, several non-idealities must be considered.

3.2.1 Design challenges

From the model in Fig. 3.1 of last chapter, the switches S_1 and S_2 have a non-zero on-resistance R_{ON} and a finite off-resistance R_{OFF}. R_{OFF} can be maximized

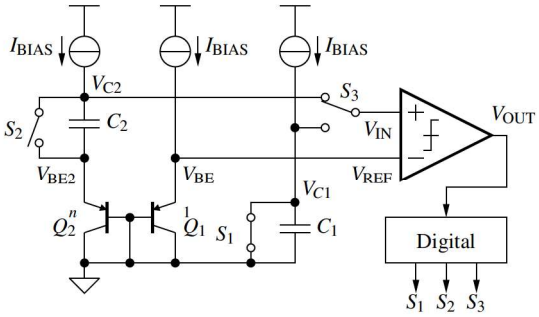


Fig. 3.1 The complete model from Fig. 2.25.

with minimum transistor dimensions, but this increases R_{ON} and causes non-zero initial voltages across C_1 and C_2 in Fig. 2.25 at the beginning of each charging cycle.

If R_{ON} is built into the model, the simulation shows an increasing error with increasing R_{ON} in Fig. 3.2. The error shows a linearity to the temperature with an offset. The more R_{ON}, the more error on the negative side.

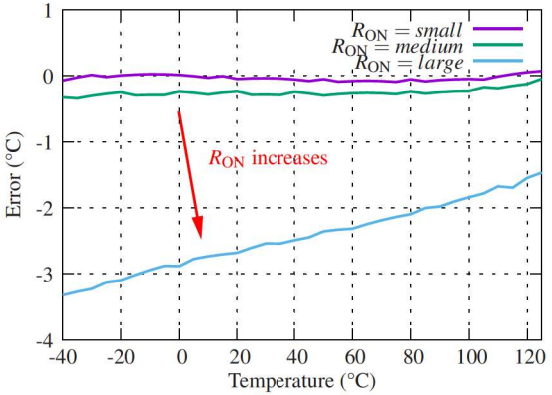


Fig. 3.2 Non-zero R_{ON} generates linear temperature error with offset.

The propagation delay of the comparator is noticeable, since the design is low-power and the comparator has to consume a low current. The delay will be fed directly into the PWM signal and further changes the duty cycle. In Fig. 3.3, the increasing propagation delay increases the gradient of the error. All the results are linear to the temperature while the curves cross at 30 °C. The reason for the crossing is that at 30 °C the nominal duty cycle is 50 %. The injected propagation delays for t_{VBE} and $\alpha t_{\Delta \mathrm{VBE}}$ in Fig. 2.27 are matched to 50 % as well. Therefore, the accuracy at 30 °C is not changed.

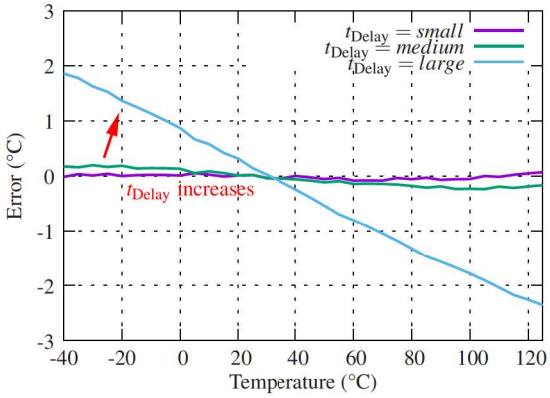


Fig. 3.3 The propagation delay of the comparator generates linear temperature error.

The offset voltage of the comparator, which is caused by process variation significantly, has a significant influence on the accuracy as well. The offset voltage affects the comparison threshold and further the timing of the PWM signal.

A comparator with increasing offest voltage is utilized for the simulation. The results in Fig. 3.4 show that the error is linear to the temperature.

Since most temperature errors are linear to the absolute temperature, linear trimming can be utilized. Since the errors show various offsets and slopes, two-point trimming is required. In Fig. 3.5, two points of the original curve

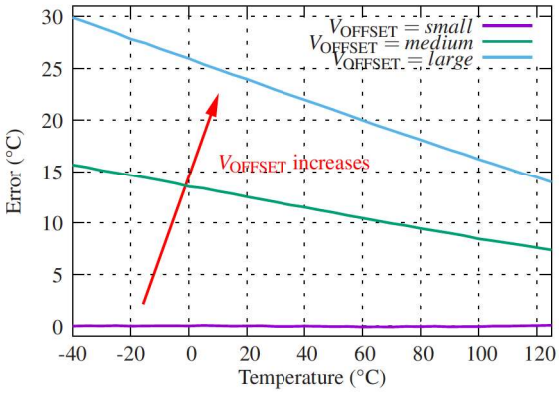


Fig. 3.4 The offset voltage of the comparator generates a linear temperature error.

are selected. By comparing the measured value and the ideal value at these two points, a first-order correction function with offset and slope is calculated. The measured curve is applied with this linear correction function, so that the measured curve is adjusted to match the ideal curve after the correction.

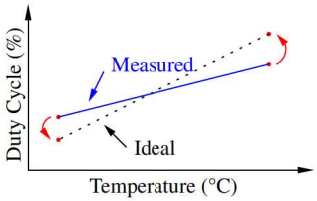


Fig. 3.5 The two-point trimming corrects the linear error caused by process variation.

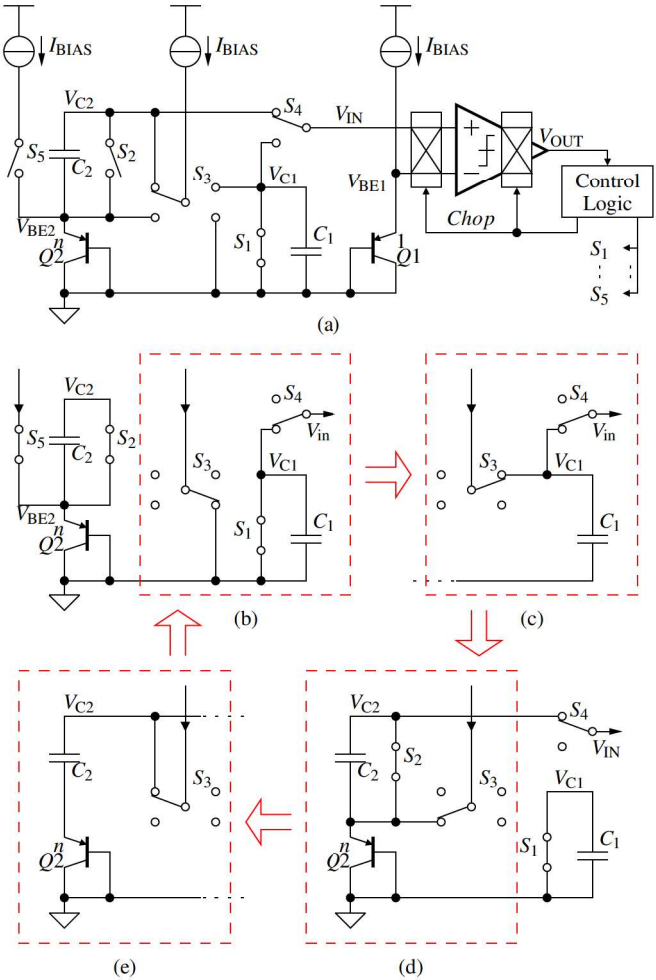


Fig. 3.6 (a) Schematic of the delay generator to cancel the non-ideal effects of the switches and the comparator and (b) (c) (d) (e) four phase switching scheme

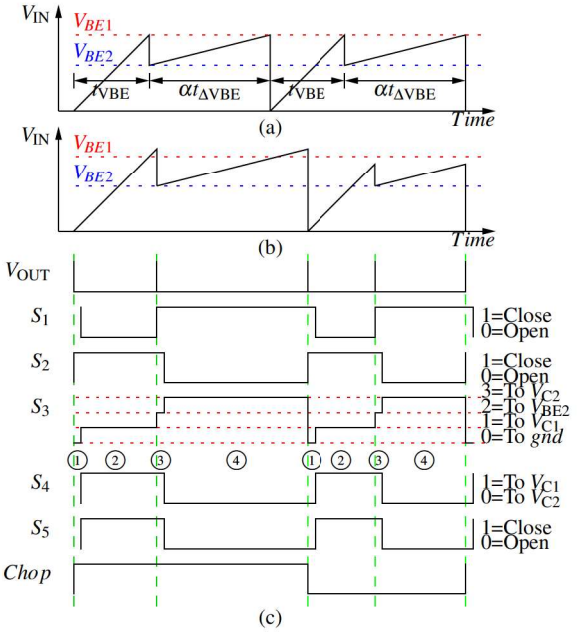


Fig. 3.7 Comparator input voltage V_{IN}: (a) ideal, (b) with offset compensation; (c) digital switch control signals: ① reset phase, ② charging phase of C_1, ③ reset and sampling phase of V_{BE2}, ④ charging phase of C_2

3.2.2 Delay generator CMOS implementation

Fig. 3.6 (a) shows the implementation of the proposed delay generator. In contrast to Fig. 2.25, I_{BIAS} can be connected to one of the four nodes V_{C1}, V_{C2}, V_{BE2} and GND via switch S_3, so that C_1 and C_2 are charged by the same current source (Fig. 3.6 (c)/(e)). Therefore, exact matching is required only for I_{BIAS} of Q_1 path and S_3 path. I_{BIAS} of S_5 path is not critical because it only serves to maintain the bias point of Q_2 (Fig. 3.6 (b)/(c)). Through S_3, I_{BIAS} flows only through one capacitor at a time while the inactive capacitor is shorted. This eliminates initial voltages across the capacitors even if R_{ON} is high. S_1 and S_2

are controlled by overlapping clocks, which makes C_1 and C_2 immune against charge injection from S_3 and S_4. At the same time, the parasitic capacitance of the comparator inputs and wires are discharged during the overlaps. The four-phase switching scheme includes a reset phase, in which the voltages inside the analog part are kept at rest before the sensor is started.

The comparator uses a chopper structure to eliminate the influence of its offset voltage V_{OFFSET} as follows. Fig. 3.7 (a) shows the waveforms that would be obtained for an ideal comparator with zero offset. The comparator signals the points in time where V_{IN} crosses the threshold set by V_{BE1} exactly. Now assume $V_{\mathrm{OFFSET}} \neq 0$. This requires V_{IN} to rise above $V_{\mathrm{BE1}} + V_{\mathrm{OFFSET}}$ to toggle the comparator, thereby increasing or decreasing t_{VBE} and $\alpha t_{\delta \mathrm{VBE}}$ proportionally, depending on the sign of V_{OFFSET} (Fig. 3.7 (b)). Due to this proportionality, the offset-induced error can be fully compensated by reversing the chopper's polarity every other cycle and computing the averages of the t_{VBE} and $\alpha t_{\delta \mathrm{VBE}}$ measurements from two subsequent cycles in the digital part.

3.2.3 Top level of the test chip

The test chip (D8001A) in Fig. 3.8 mainly consists of the time-domain temperature sensor, a bias block and a on-chip serial peripheral interface (SPI). The bias block provides a bias current, which is utilized by the delay generator. The delay generator outputs the PWM signal, which can be evaluated by external devices. The analog blocks are controlled by a digital logic, which is connected to a on-chip SPI interface. The on-chip SPI interface, which is a slave device, communicates with the off-chip master device. This allows the master device to control the internal blocks by sending commands. The signals *MOSI*, *MISO*, *SCLK* and $\overline{SS}$ are the standard SPI pins. while *CLK* provides the clock signal for the entire chip. The internal analog signals can be multiplexed and buffered by a test structure for the measurement purpose.

In the top-level simulation the inaccuracy of this temperature sensor is evaluated. In the Monte-Carlo simulation, the temperature sensor is simulated in 50

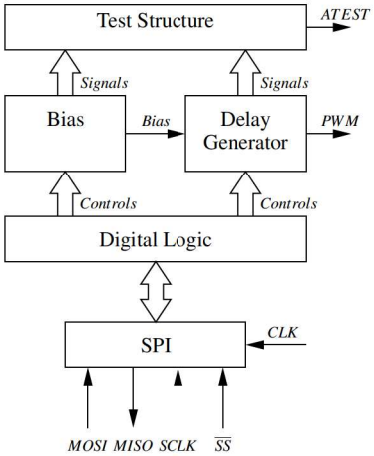


Fig. 3.8 Test chip of the proposed temperature sensor

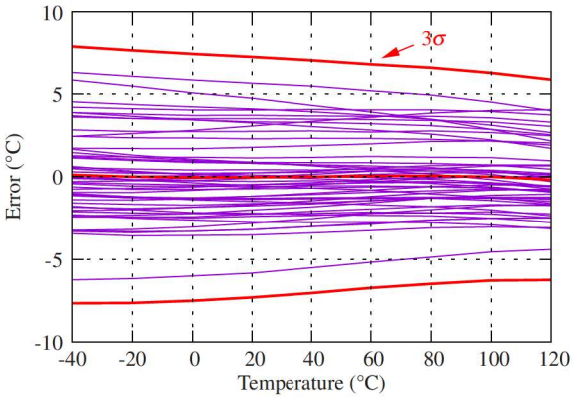


Fig. 3.9 The untrimmed simulation inaccuracy is in the range of ±8 °C (3σ).

times. Each time random parameters with normal distribution are assigned to each component of the temperature sensor. In this way, the distribution of the final results can be examied before tape-out.

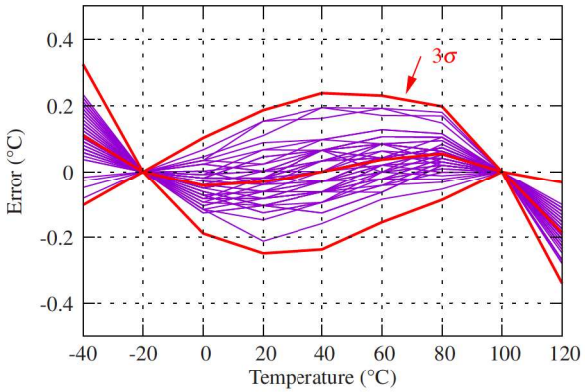


Fig. 3.10 After two-point trimming the inaccuracy is reduced to ±0.4 °C(3σ).

Without trimming, the absolute error is spread in the range of approximately ±6 °C from −40 °C to 120 °C. The mean inaccuracy at each temperature step is approximately located around 0 °C. The three times stand deviations (3σ) of the error, which represents 99.7 % of the error possibility, are under ±8 °C.

Two-point trimming is performed at −20 °C and 100 °C. After trimming the residual error shows an obvious third-order property in [-0.2,0.1] °C, which means the second-order error is already eliminated. The standard deviation is significantly reduced with 3σ of ±0.4 °C.

3.2.4 Experimental results

Chip photo and measurement setup

The temperature sensor was implemented in a commercial 0.35 µm CMOS technology with four metal layers and low-Vt option (Fig. 3.11). The delay generator and digital logic use active areas of 0.87 mm^2 and 0.08 mm^2, respectively. The capacitor array uses 0.55 mm^2, which is required for a PWM period that is long enough to achieve the desired accuracy.

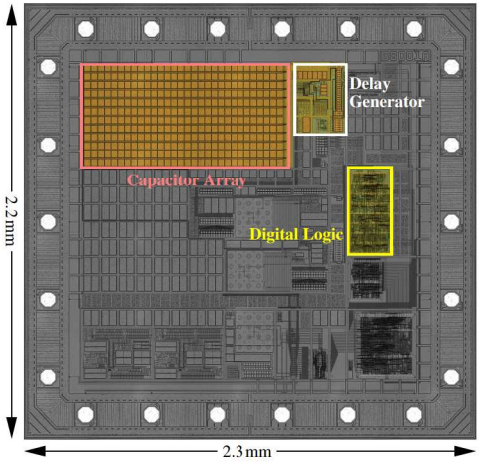


Fig. 3.11 Photography of the test chip

At room temperature, the delay generator draws 1.5 µA from a 1.4 V power supply. Not counting the current contributions from any peripheral logic components on the test chip, such as serial data interfaces, the intrinsic digital part of the sensor consumes approximately 1 µA. The conversion time for one sample is 1.16 ms, corresponding to the PWM period length.

Fig. 3.12 shows the precision measurement assembly used to determine the absolute temperature error and trim the device. The assembly utilizes Chip-on-Board (CoB) technology, which bonds the chip directly to a printed circuit board (PCB). The sensor is glued on top of a PT1000 reference resistor. The entire assembly is placed in a tube under a Thermostream nozzle in Fig. 3.13. The outputs of the PT1000 device and the CMOS sensor were recorded simultaneously while the air temperature was varied automatically from –40 °C to 125 °C in steps of 5 °C. Each step was held for 60 s to establish thermal equilibrium inside the device under test before acquiring the readings.

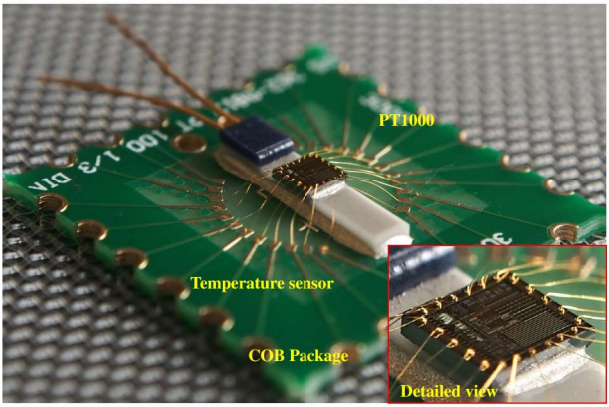


Fig. 3.12 The CoB package is utilized to let sensor operate with PT1000 in a closed junction.

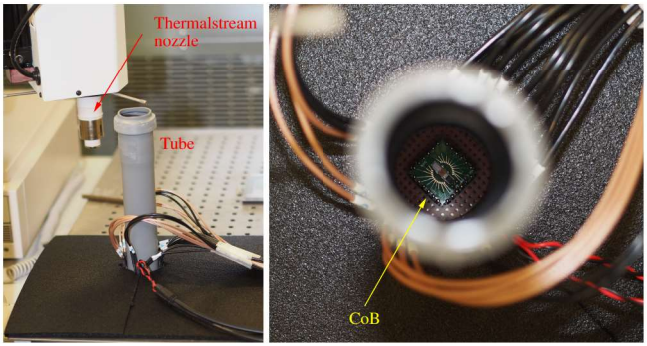


Fig. 3.13 (a) The Thermostream nozzle blows cold/hot air for controlling the temperature in the tube. (b) The top view of the tube

Sensing accuracy

Fig. 3.14 shows the measured absolute error before trimming, which is in the range from 2 °C to 9 °C. Following the temperature sweep, the raw sensor data

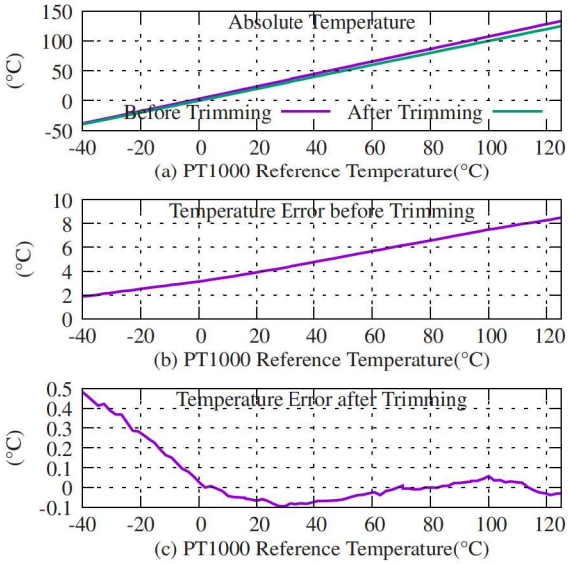


Fig. 3.14 Measurement results (a) absolute temperature before and after trimming; (b) error before trimming; (c) error after trimming

was corrected using two-point trimming. After trimming the correction function at 0 °C and 80 °C using the corresponding PT1000 readings, the CMOS sensor achieves an absolute error of −0.1 °C to 0.5 °C in the full temperature range from −40 °C to 125 °C and ±0.1 °C in the range from 0 °C to 125 °C. The overall resolution is 0.3 °C, limited mainly by thermal and flicker noise from the bias source and the switches. A summary and comparison of the performances is given in Table 3.1.

Table 3.1 Performance Summary and Comparison

Parameter	**This work**	[23]	[12]	[37]
CMOS process [μm]	**0.35**	0.18	0.35	0.16
Sensing domain	**Time**	Time	Time	Voltage
Calibration method	**Digital**	Digital	Digital	Digital
Calibration points	**2**	2	2	1
Temp. range [°C]	**−40...125**	−20...30	0...90	−55...125
Supply voltage [V]	**1.4**	1.0	3.3	1.5
Supply current [μA]	**2.5**	0.1	11.1	3.4
Inaccuracy °C	**−0.1/0.5**$^{(1,3)}$ **±0.1**$^{(2,3)}$	±0.8$^{(4)}$	−0.25/ 0.35$^{(3)}$	±0.15$^{(4)}$
Resolution °C	**0.3**	0.2	0.0918	0.02
Conversion time [ms]	**1.16**	40	500	5.3
Energy per conversion [nWs]	**4.1**	4.0	1.8×10^4	27

(1) Temperature range −40 °C to 125 °C
(2) Temperature range 0 °C to 125 °C
(3) Min, max inaccuracy
(4) 3σ inaccuracy

3.3 RFID implementation

3.3.1 PMU implementation

The implementation of this RFID PMU consists of the rectifier, the voltage reference, the LDO and the voltage limiter.

Rectifier

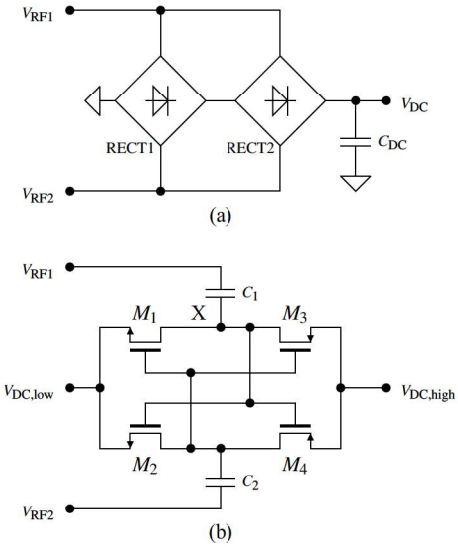


Fig. 3.15 The overall 2-stage rectifier design (a) and stage design (b).

The core structure consists of conventional two-stage cross-connected differential rectifiers [26, 40, 4, 67, 21]. The single stage in Fig. 3.15 (b) shows that the transistor pairs M_1, M_4 and M_2, M_3 are alternately switched on, when V_{RF2} and V_{RF1} are alternately high, respectively. The DC voltage $V_{DC,high}$ is generated approximately the sum of the DC voltage $V_{DC,low}$ and the AC amplitude, when the rectifier drives no load. The DC voltage $V_{DC,high}$ decreases, when loads are presented at the output. The more current load presents, the less voltage $V_{DC,high}$ is generated. If the output DC voltage is not high enough, the multiple stages can be stacked to achieve a higher voltage. In Fig. 3.15 (a), this design utilizes two stages to achieve approximately twice the AC amplitude. The capacitors C_1 and C_2 are used to boost the AC common-mode voltage for the second stage.

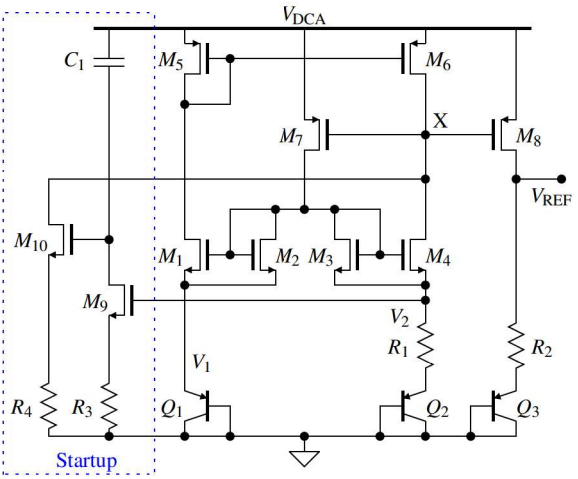


Fig. 3.16 The block diagram of the bandgap reference.

The smoothing capacitor C_{DC} is used to stabilize the DC voltage when the AC waves are in phase transition.

Voltage reference

Compared to [76], this design requires a low-power voltage reference without trimming, since the absolute value of the supply voltage is not decisive. The schematic of the bandgap reference is shown in Fig. 3.16. The diode-connected bipolar transistors Q_1 and Q_2 and the resistor R_1 are the bandgap core for generating the PTAT current. M_1, M_2, M_3, and M_4 form the current-input amplifier, which takes the currents of Q_1 and Q_2 as input currents and passes the currents to the current mirror M_5 and M_6. At the high-impedance node "X" the gate voltage of M_7 is built by the large output resistance and the differential current of M_4 and M_6. The transistor M_7 regulates the current to the current-input amplifier and further regulates the currents through Q_1 and Q_2 until the voltage V_1 equals V_2. The generated PTAT current is mirrored to M_8. Finally, the reference

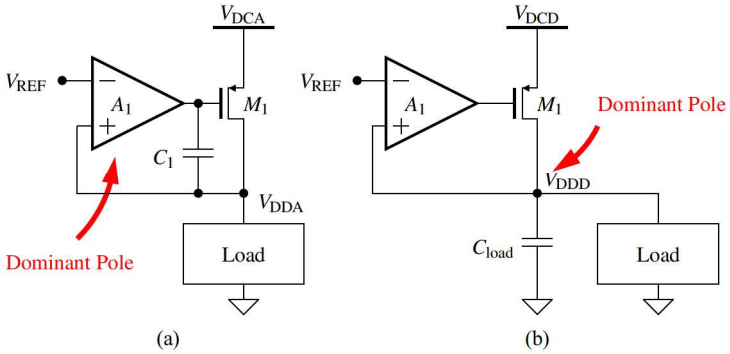


Fig. 3.17 The block diagram of LDO for (a) analog load and (b) digital load.

voltage V_{REF} is generated by the PTAT current, R_2, and D_3. The startup circuit is formed by $M_{9,10}$, $R_{3,4}$, and C_1, which detect the voltage V_2 and pull a startup current from the node "X".

Low-dropout regulator

The LDO connected to V_{DCA} generates the regulated supply voltage V_{DDA} for the temperature sensor. Since this LDO supplies only chip-internal low-power blocks, it must be a low-power implementation as well. For analog load and digital load, two different design strategies are used in Fig. 3.17.

Since the on-chip analog load can be predicted very well, the pole of the output stage can be calculated. Therefore, the dominant pole (Fig. 3.17 (a)) can be designed on the error amplifier, so that the power consumption of the analog LDO can be minimized. On the other hand, the digital logic generates large dynamic current spikes during the transition, so the large capacitor C_{load} is needed to smooth the voltage drops (Fig. 3.17 (b)). With large C_{load}, the pole of the output stage becomes the dominant pole, so the error amplifier must be relatively fast.

Voltage limiter

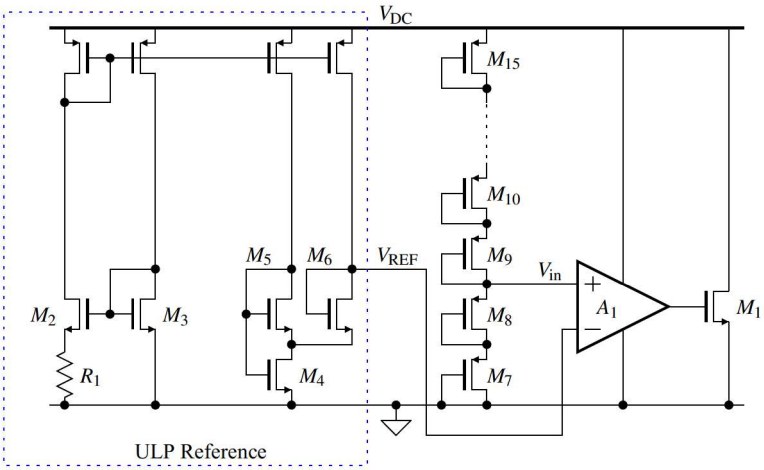


Fig. 3.18 The block diagram of the voltage limiter

If the incoming power is too high, the rectified DC voltage V_{DC} may exceed the maximum allowable supply voltage of the CMOS process. In this 0.35-µm technology, the voltage is limited by 3.6 V. The principle of this circuit is shown in Fig. 3.18. The DC voltage is scaled down to a lower voltage, so that it can be passed to an OpAmp A_1. On the other hand, A_1 takes the reference voltage as the negative input. The OpAmp A_1 regulates the NMOS transistor M_1, so that M_1 can bypass the additional current. The voltage V_{in} is generated by a voltage divider consisting of 9 diode-connected PMOS transistors $M_7..M_{15}$. The reason for implementing PMOS transistors instead of large resistors is to save current and chip area, since the current through this path should be as small as possible.

3.3.2 RFID frontend implementation

The RFID frontend consists of a demodulator, a modulator, and a clock recovery circuit [13, 24, 67]. The demodulator converts the modulated RF signal to a

digital bitstream, while the modulator modulates the response to the carrier signal. The clock recovery module extracts the RFID carrier frequency and scales it down to a lower frequency for system operation.

Demodulator & Modulator

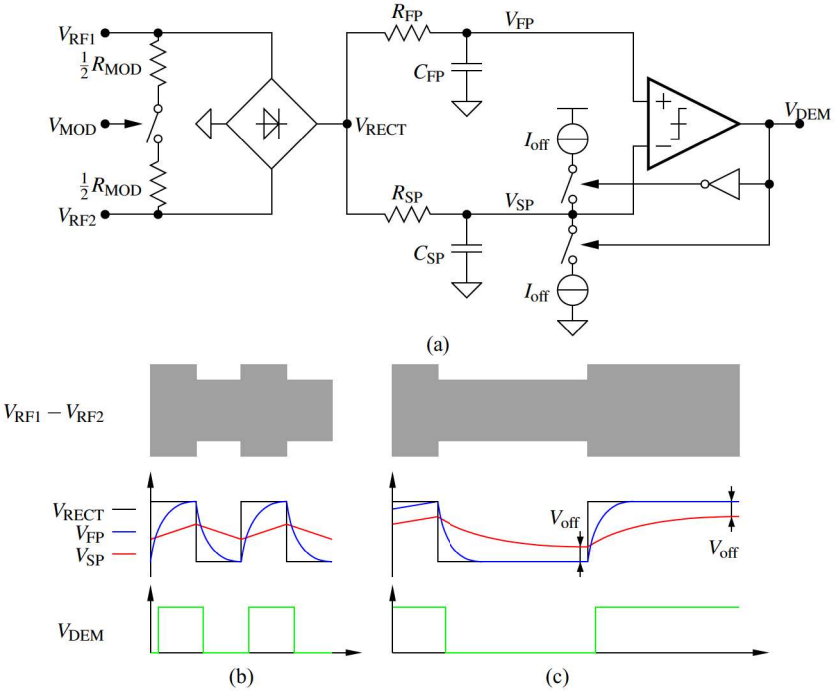


Fig. 3.19 The design of the demodulator and modulator (a) and the signal diagram for the case of fast changing (b) and slow changing (c) [67]

The demodulator operates with a modulation depth between 85.2 % and 75.4 % [73]. Some demodulators utilize a high-pass filter for the rectified voltage to capture the rising edge and the falling edge [24]. However, the detection is limited by the signal amplitude and the comparator offset. In this design, a

demodulator in Fig. 3.19 (a) is developed for small amplitude. A rectifier operates as an envelop detector and outputs V_{RECT}. R_{FP} and C_{FP} form a fast signal path, whose cutoff frequency is approximately 200 kHz. The fast path signal V_{FP} can easily track V_{RECT} in one elementary time unit (ETU) [73], which is approximately 9.44 µs. On the other hand, R_{SP} and C_{SP} form a slow signal path, whose cutoff frequency is approximately 2.4 kHz. A comparator is utilized with V_{FP} and V_{SP} as two input signals to generate the digital output signal V_{DEM}. Between V_{RF1} and V_{RF2} a shunt path is formed as a modulator, so that the current can be controlled by V_{MOD}. Switching the resistor R_{MOD} on and off can result in different impedances, that can be coupled to the reader coil and detected by the RFID reader.

In Fig. 3.19 (b), if the bit stream changes rapidly, the reference voltage V_{SP} can maintain relatively constant in the middle. V_{FP} reaches rail-to-rail in an ETU, so that V_{DEM} can generate the proper rising/falling edges. If the bit stream maintains unchanged in multiple ETUs, V_{SP} can slowly reach the rail. The comparator, which normally has an input offset voltage, could make a wrong decision on V_{DEM}, so that V_{DEM} could represent the wrong command. To solve this problem, two small current sources in Fig. 3.19 (a) are added to the slow path. They are controlled by V_{DEM} to create a manual positive or negative offset voltage V_{off}. In Fig. 3.19 (c) the voltage V_{SP} no longer reaches the rail, but reaches a higher or lower voltage if V_{DEM} is low or high, respectively.

Clock recovery

The clock recovery extracts the carrier frequency and further scales it down fourfold to generate the system clock. In the design [67], the voltage V_X in Fig. 3.15 (b) is utilized to drive an inverter to extract the carrier frequency. A cross latch is formed by inverter and positive feedback [13] to divide the input frequency by 2. Two cross latches are used to generate the system clock frequency of 3.39 MHz.

3.3.3 RFID simulation results

PSR simulation

The voltage reference, analog LDO and digital LDO are simulated for power supply rejection. The AC voltage sources are given to the nodes V_{DCA} and V_{DCD} in Fig. 2.1. The AC responses of V_{REF}, V_{DDA} and V_{DDD} are measured so that the PSR of the reference, the analog power path and the digital power path can be analyzed, respectively.

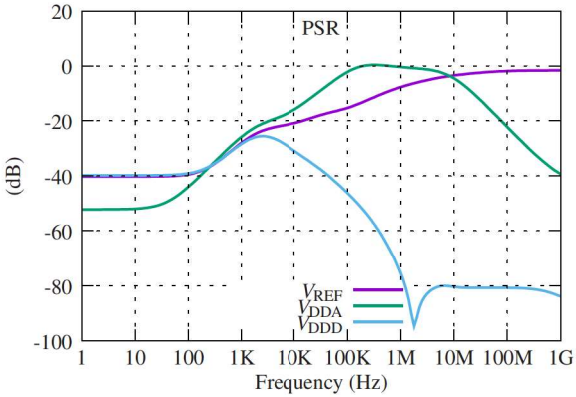


Fig. 3.20 The PSR of voltage reference (V_{REF}), analog power path (V_{DDA}) and digital power path (V_{DDD}).

The three results in Fig. 3.20 show different AC responses. The PSR of V_{REF} starts with approximately –40 dB. In the modeling, we learned that the PSR will drop at high frequency (10 MHz to 1 GHz in Fig. 2.12). However, in this case from approximately 100 Hz to 1 GHz, the PSR increases slowly to –2 dB. The reason is that the modeling did not cover this case, which consists of a single common-source output stage. In Fig. 3.16 the output stage is not within the regulation loop. Therefore, the noise of this power path is directly added to the output. The node X in Fig. 3.16 has approximately 0 dB PSR in the frequency domain due to topology. Since the reference output node V_{REF}

has a very small parasitic capacitor to ground, the C_{ds} of M_8 dominates. As the frequency increases, more parasitic current is applied to the load, so that PSR_{ref} increases to approximately 0 dB.

For the analog power path and digital power path, the simulation results show similarity to the previous models. The peak PSR of analog power path is approximately 0 dB, while the peak PSR of digital power path is approximately –25 dB.

In the transient simulation, a 50 kHz pulse between 2 V and 2.2 V is given on V_{DC}. The output voltage V_{DDA} shows a ripple with a peak-to-peak amplitude of 345 mV, while V_{DDD} outputs a ripple with a peak-to-peak amplitude of 374 μV. Since the LDO operates in a wide dynamic range at the rising/falling edges, and the pulse occupies large bandwidth in the frequency domain, the amplitude of the ripple is larger than the theoretical value.

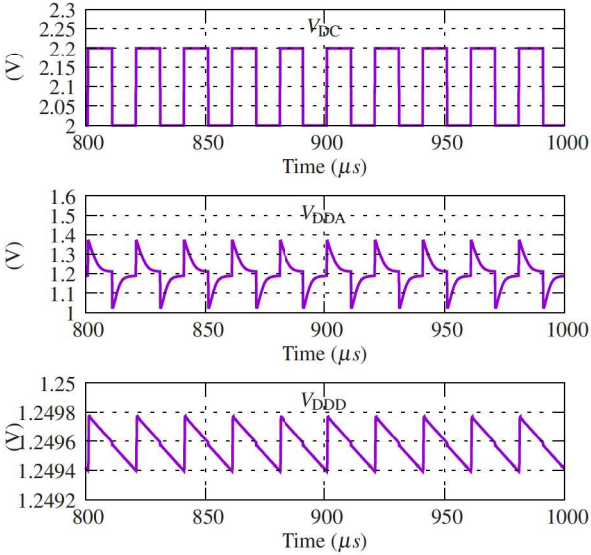


Fig. 3.21 Transient responses of V_{DDA} and V_{DDD} with 200 mV pulse input.

System transient simulation

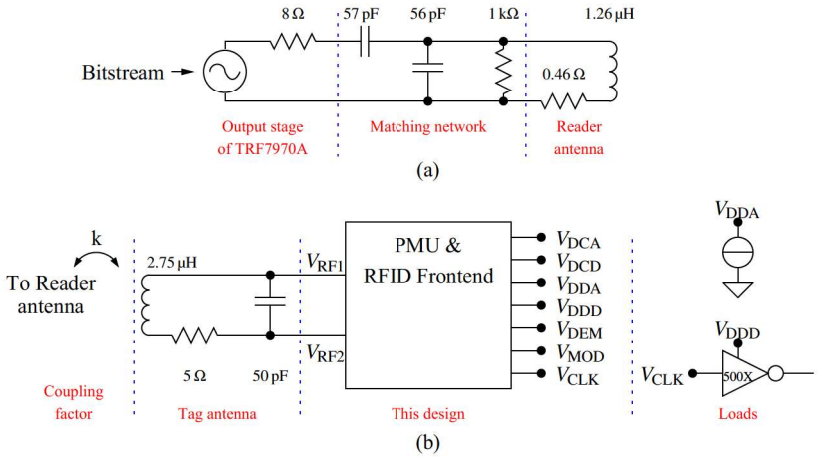


Fig. 3.22 Testbench of the PMU and the frontend

The testbench utilizes *Texas Instruments TRF7970A* [81] as RFID reader to obtain convincing simulation results. *TRF7970A* integrates an RFID analog frontend and a multi-protocol engine, which supports most of the commercial HF RFID standards. The *evaluation module of TRF7970A* [82] is the reader system built by *TRF7970A* and other necessary components to demonstrate the funtionalities of *TRF7970A*. This evaluation module is utilized to measure the entire RFID sensor tag, so it makes sense to model it in the simulation environment. The modelling in Fig. 3.22 includes:

- the on-board reader antenna,
- the on-board matching network for reader antenna,
- the configurable RF output power of *TRF7970A*,
- the coupling factor, which indicates the geometry of the both reader/tag antennas and the relationship between them,

- the tag antenna,
- and the loads that emulate the current consumption of the sensor and the digital logic.

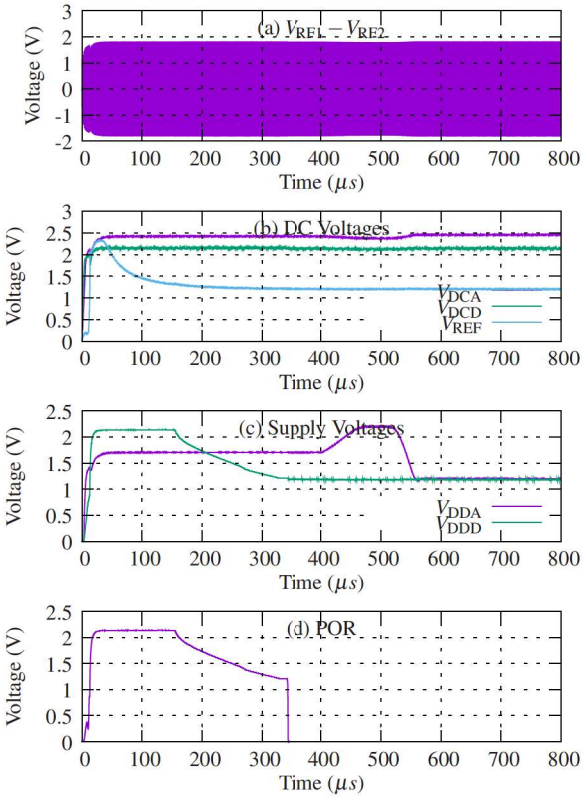


Fig. 3.23 During startup, the simulation results of (a) RF inputs, (b) DC voltages, (c) supply voltages and (d) the power-on-reset.

Firstly, the startup process is simulated. From 0 µs, the RF field is energized so that the RF signal $V_{RF1} - V_{RF2}$ starts to oscillate and reaches peak-to-peak

amplitude of ±1.8 V. The rectifiers start to operate and reach sufficient voltages at approximately 30 µs. With sufficient V_{DCA}, the bandgap voltage reference starts to regulated itself to the desired voltage (1.2 V). After approximately 200 µs, the reference approaches 1.2 V, so that the analog LDO and the digital LDO begin to regulate. The digital LDO generates the desired V_{DDD} at 350 µs, while the analog LDO finishes the regulation at about 560 µs. The reason, that the digital LDO is settled differently as the analog LDO, is because the error amplifier of digital LDO has a larger bandwidth. The power-on-rest (POR) signal starts from the beginning and ends at 340 µs for resetting the digital logic. The entire startup process finishes when V_{DDA} is settled. After approximately 600 µs, the chip is ready to take commands.

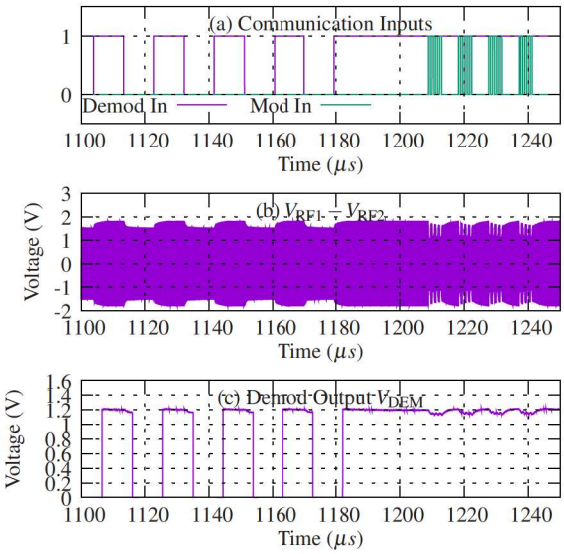


Fig. 3.24 During communication the simulation results of (a) RF inputs, (b) unregulated DC voltages and (c) supply voltages

The RFID communication is sent after 1 ms. The reader-to-tag communication uses 9.44 µs (106 kHz) as Elementary Time Unit (ETU) according to

the protocol definition. The tag-to-reader communication uses 848 kHz signal modulated on a 106 kHz sub-carrier signal. In Fig. 3.24 (a), the communication inputs are given from the testbench. The amplitude modulation is clearly shown on the RF carrier signal in Fig. 3.24 (b). In Fig. 3.24 (c), the RFID frontend demodulates and generates the digital signal for the digital logic, which is shifted by a certain time. This is because the demodulator works relatively slowly with low current consumption. Since the demodulator reconstructs the input communication bitstream, the timing delay is not crucial.

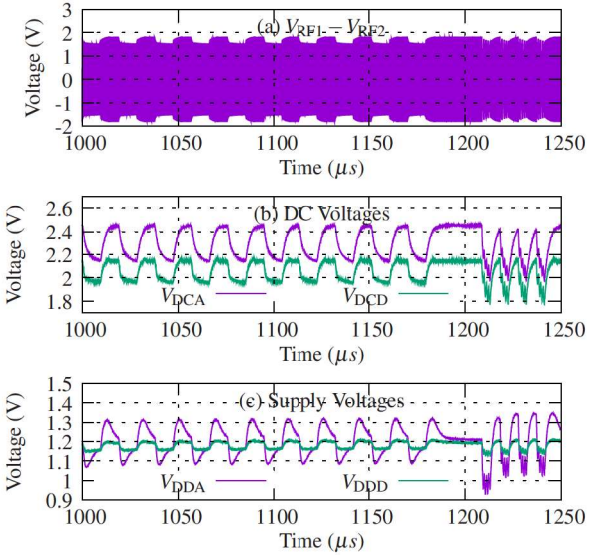


Fig. 3.25 During communication the simulation results of (a) RF input, (b) unregulated DC voltages and (c) supply voltages

During communication in Fig. 3.25, the RF amplitude changes with approximately 85 % modulation depth. This generates voltage ripples on both V_{DCA} and V_{DCD}. During reader-to-tag communication, the modulation induces 295 mV and 207 mV at V_{DCA} and V_{DCD}, respectively. Accordingly, V_{DDA} and

V_{DDD} show 224 mV and 66 mV ripples, which represents PSR of −2.4 dB and −10 dB, respectively. The PSR of the analog power path matches relatively to the AC PSR simulation results, while the digital power path produces large variations. The reason for this is that the digital circuits are taken into account in the transient simulation. Since the digital switching consumes power provided by the LDO pass transistor, the bandwidth of the LDO output stage is dynamic increased. This leads to the degradation of PSR at the communication frequency. Furthermore, the digital current spikes pull V_{DDD} dynamically with a large amplitude, which enhances the PSR degradation. The larger the digital logic in the overall system, the greater the ripple generated on V_{DDD}. For the tag-to-reader communication in Fig. 3.25, similar conclusion can also be obtained.

3.4 Summary

In this chapter the mixed-signal circuit implementation of the temperature sensor and RFID is presented.

The CMOS implementation of the temperature sensor brings further design challenges, e.g. non-zero R_{ON} and finite R_{OFF} of the switches, the propagation delay of the comparator, the offset voltage of the comparator. These effects ruin the sensor accuracy considerably, so that several design techniques are utilized. A chopper structure is utilized to eliminate the offset voltage of the comparator. A four-phase switching scheme is implemented for the non-idealities of the switches. To compensate the propagation delay of the comparator, the main capacitors are chosen as large as possible, so that the delay can be neglected. The residual errors caused by process variation are corrected by two-point trimming. The experiment results show that the inaccuracy of the temperature sensor achieves −0.1 °C to 0.5 °C in the entire temperature range from −40 °C to 125 °C and ±0.1 °C in the range from 0 °C to 125 °C, while the resolution is 0.3 °C.

The RFID implementation consists of rectifier, bandgap, LDO, limiter, demodulator, modulator and clock recovery. The simulation of the PMU includes

the PSR analysis of the analog/digital power path and the transient analysis of startup and RFID communication. During reader-to-tag communication, the PMU shows ripples of 224 mV and 66 mV on V_{DDA} and V_{DDD}, respectively. These result correspond to a PSR of −2.4 dB and −10 dB on analog power path and digital power paths, respectively.

Chapter 4

System integration and physical design

4.1 Introduction

In the previous chapters, the temperature sensor and the wireless RFID design are introduced. System integration can be achieved by combining the temperature sensor and RFID in one system and ensuring that the two main sub-blocks are not interfered with each other. In addition, the interface between two blocks must be defined and designed completely so that the cooperation between them is not compromised. Finally, a central control block is required to organise the operations of the analog blocks.

In detail, many new challenges are revealed at the system level. First, the output interface of the temperature sensor must be adapted. The sensor is powered by the PMU, while its output (PWM signal) has to be digitized. In addition, the components can be combined in many ways. In terms of the communication protocol, some designs [43] utilize the commercial protocol, while others [25, 10, 9, 36] use the customized protocol. In [36], the smart sensor output

is converted into a PWM signal, which is modulated directly via RF, so that the design complexity can be reduced. However, the chip is no longer compatible to the commercial reader. For the overall system, some solutions [80, 58, 54, 50] bring the components together on the PCB, while some designs [90, 36, 43] integrate the most important components on chip for system-on-chip (SoC). In the end, the temperature sensor must be considered clearly in the RFID environment. The previous chapters prove that the temperature sensor accuracy is significantly affected by supply interference, which is not avoidable in a typical RFID PMU design. In [7], this effect is already observed, but was barely discussed in the paper. Therefore, a solution for improving sensor accuracy in the system level is essential.

In this design, a standard ISO/IEC 14443 type B protocol with physical layer is utilized to ensure basic compatibility with commercial readers. To reduce power consumption and design effort, the communication layer is simplified so that the commercial reader only requires a software update to work with this tag. All components are integrated on one chip to achieve the system-on-chip (SoC) target, so that the overall system is miniaturized. A new RFID command is introduced so that the temperature sensor can avoid the period of strong supply interference.

This chapter is organized as follows. In section II, the system level optimization is presented. The sub-blocks are integrated on a SoC in section III. The physical design and conclusions are shown in section IV and section V, respectively.

4.2 System level optimization

4.2.1 Communication protocol

This work employs a very simple internal communication protocol for providing a faster and power efficient design. The main purpose of the design is not to fulfill the design standards prescribed for RFID tags, but to develop a power

efficient, faster and low cost application [78]. Since the physical layer follows ISO/IEC 14443 type B protocol, the communication eliminates the initialization and anti-collision for saving energy and simplifying the design effort. In this design, the communication utilizes a direct access for polling commands. Two fundamental commands are realized: Readout command and write command.

Readout command

Fig. 4.1 Communication frame from reader to tag of readout includes ①: SOF, ②: Tag ID, ③: Command ID, ④: Memory address and ⑤: EOF.

The readout command allows a RFID reader to read 4 bytes continuously from the internal memory. In Fig. 4.1 the Readout command has following fields:

1. Start of frame (SOF) indicates the start of the command.
2. Tag ID specifics the 2-byte identification number of the tag.
3. The Command ID is "03" in this case.
4. Memory address specifics the start address to be read.
5. End of frame (EOF).

In Fig. 4.2, The response of the readout command has following fields:

1. TR1 is the synchronization time to let the reader lock the tag response.
2. Start of frame (SOF) indicates the beginning of the response.

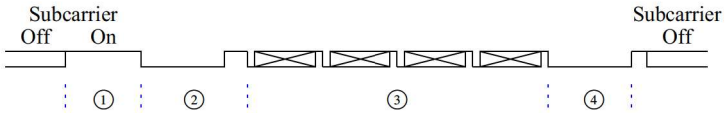


Fig. 4.2 Communication frame from tag to reader of readout includes ①: TR1, ②: SOF, ③: Data, ④: EOF

3. Data contains 4-byte information.
4. EOF indicates the end of the response.

Write command

The write command allows a RFID reader to write one byte to the internal memory. Write command has following fields:

1. Start of frame (SOF) indicates the start of the command.
2. Tag ID specifics the 2-byte identification number of the tag.
3. Command ID is "02" in this case.
4. Memory address specifics the address to be written.
5. Data contains one-byte information.
6. End of frame (EOF).

The response of the write command has following fields:

1. TR1 is the synchronization time to let the reader lock the tag response.
2. Start of frame (SOF) indicates the beginning of the response.
3. Acknowledge contains 2-byte tag ID.
4. EOF indicates the end of the response.

4.2.2 Serial readout command

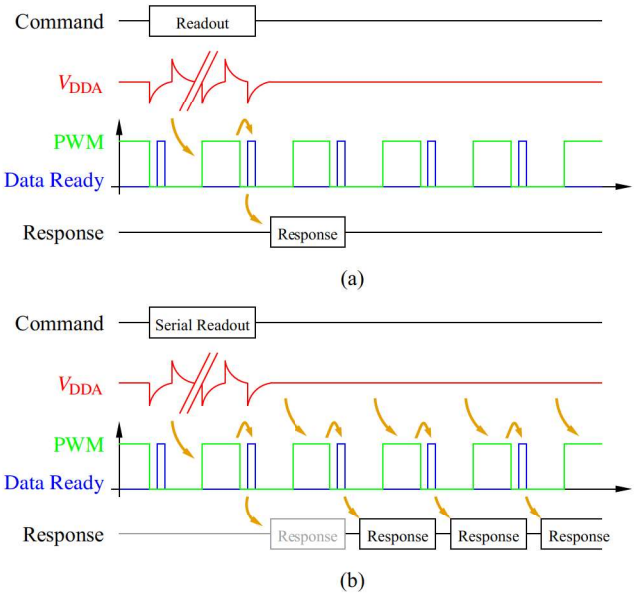


Fig. 4.3 Signal waveforms of readout command and tag response from (a) standard readout and (b) serial readout.

Due to the high sensitivity of the temperature sensor to supply interference, a system-level solution has been developed for enabling a single command to cause a series of measured values to be recorded and transferred. Fig. 4.3 shows for two cases the timing relationships between the readout command, the noise in the supply voltage (V_{DDA}), the sensor output (PWM, Data Ready) and the response from the RFID sensor tag. The two cases are standard readout (Fig. 4.3 (a)) and serial readout (Fig. 4.3 (b)). When the standard readout command is sent, the temperature information is returned in one action to the reader. In contrast, after the serial readout command a number of sets of temperature data are returned to the readout device. In both cases, the temperature sensor

had already been switched on before the readout command came, as is revealed by the activity of the PWM signal shown in green. Each time measurement has been completed and there is a new measured value ready for transfer, the signal "Data Ready" is shown.

Fig. 4.3 (a) shows how the transfer of the standard readout command distorts the measured value that is to be sent next. The noise generated on the supply voltage V_{DDA} while the measurement is being taken leads to an error in the rising edge of the PWM signal which alters the ratio. Thus, in the case of single readings using the standard readout method, the response from the RFID temperature detector is always affected by the interference.

Fig. 4.3 (b) shows the response to a serial readout command requiring several sets of data to be sent one after the other to the reader. Here it is clear that the data arriving after the second response is not affected by the voltage interference due to the readout command because there is no HF communication coming at that time from the reader. There are still errors after the second response because of supply noise generated by the communication from the tag while it responds, but this noise has much less effect on the measurement. Furthermore, the RFID reader is capable of applying an averaging procedure to series of values transferred, reducing the residual inexactitude so much that it barely affects the measuring accuracy of the complete system.

4.3 System integration

4.3.1 Time-to-digital converter

Since the temperature sensor outputs a PWM signal, which can not be transmitted directly via RFID, a time-to-digital converter (TDC) is needed. TDC is used in various application scenarios, e.g. time-of-flight laser range-finding [33, 34] and all-digital frequency synthesis [38]. In this application, a TDC with low-power, simplified topology and relaxed resolution is implemented. This TDC

utilizes an asynchronous counter for asynchronous measurement, which provides low-power and a wide linear range.

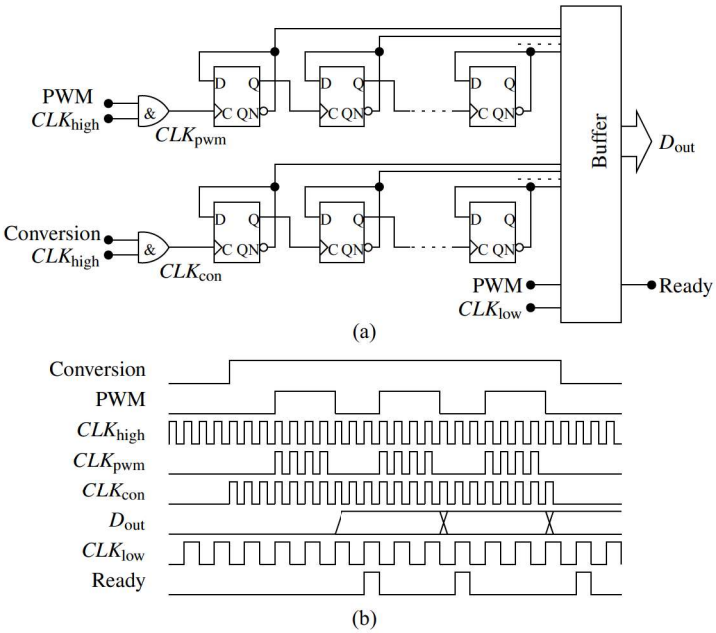


Fig. 4.4 (a) The TDC utilizes two counters for period and pulse, and (b) the simplified signal diagram

To obtain the temperature, the duty cycle must be calculated. Since the duty cycle needs two parameters: period and pulse width, two counter paths are implemented. In Fig. 4.4 (a), a high frequency clock CLK_{high} (see Fig. 4.4 (b)) is given as input and filtered by PWM and conversion, which represent pulse width and period, respectively. The two filtered clock signals CLK_{pwm} and CLK_{con} are sent to two asynchronous counters, which is created by D flip-flops. A buffer is utilized to capture the correct digital codes and transmit them to the output D_{out}. A control signal "Ready" is generated after D_{out} is refreshed to notify next stage

that D_{out} can be readout. The "Ready" signal utilizes a slow clock CLK_{low} in order to save power.

4.3.2 Digital control logic

Fig. 4.5 shows the simplified digital architecture of this passive HF RFID tag. The digital block is comprised of a protocol engine for decoding of the received data and encoding the transmitted data, a wishbone interface for on-chip communication between different modules, a control block for data processing, a register array for storing configuration bits and a clock management block for dynamically controlling the power consumption of the digital block. The main functionality of the digital block consists of receiving the demodulated information from the analog frontend and performing the decoding and command operation. Once the information is processed, the data is modulated back to the reader. The digital communication protocol is compatible with ISO/IEC 14443 Type B (Part-2).

Since the tag is intended for passive operation, reducing the dynamic power consumption of the digital block is vital. The clock management (CM) block helps to achieve this. The CM block controls the operation of the internal digital block adaptively and dynamically so that the power consumption of the digital block can be reduced significantly. When the tag operates in the receiving state, only the decoder block is activated and all the remaining blocks are turned off. Once the information has been decoded successfully by the decoder, the received information is processed in the control block. During this period, the decoder and encoder blocks are not operational. Finally, the encoder block is activated to encode the data and transmit it back to the reader by load modulation.

4.3.3 System schematic

Finally, the schematic of the top level is shown in Fig. 4.6.

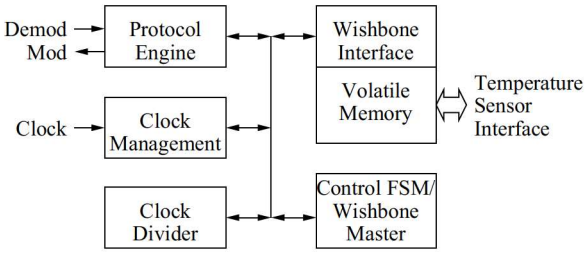


Fig. 4.5 Block diagram of digital logic

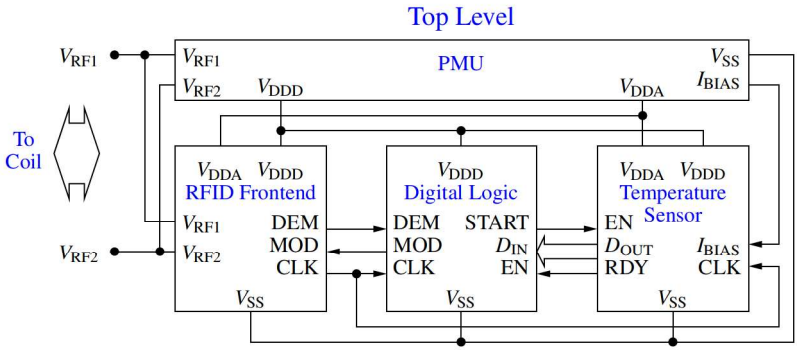


Fig. 4.6 The top level design integrates all the sub-blocks.

4.4 Physical design

The chip is a mixed-signal design consisting of both analog and digital parts. The fundamental layout techniques [3] are used so that the chip performance does not drift significantly. To obtain a good matching, the matched devices are placed close together. The matched devices are separated and mixed by interdigitation and common centroid placement. The dummy devices are added at the boundaries to ensure that the parasitics of each component are equal. The shielding is also utilized to protect the noise-sensitive analog signals. Since the chip is a mixed-signal design that includes power supply generation, a relatively

large digital logic block and noise-sensitive analog sensors, the layout must be carefully designed in terms of noise.

4.4.1 Floorplan

The floorplan plays a critical role in the layout design for noise consideration. In Fig. 4.7 (a) the sub-blocks can be categorized into three types. Firstly, the analog block of the temperature sensor is noise sensitive block, which defines the sensor accuracy. The bandgap voltage reference is also a noise sensitive block, since the reference voltage must be stable for the rest of the chip. On the other hand, most of the noise comes from the digital logic block, since this digital logic has a complicated functionality and occupies a relatively large area. Besides that, the clock recovery and demodulator/modulator can be considered as noise generation blocks as well. Finally, the mixed-signal interface connects the noise-sensitive and noise generation blocks. In temperature sensor, the SC interface, which is the bridge between analog block and the digital controls, is one such block.

To reduce the noise conduction from noise generation blocks to noise sensitive blocks as much as possible, they have to placed far apart. Considering the limited chip area, they normally take two opposite corners. The rest of the sub-blocks, which are less sensitive to the noise, can be used to fill the gap. The analog blocks, e.g. the analog part of the temperature sensor and the SC interface, utilize V_{DDA} as power supply, while the digital blocks utilize V_{DDD} as power supply. To implement the layout easily, the analog and digital LDOs should be built near analog and digital blocks, respectively. Similar to the LDOs, the analog and digital rectifiers are implemented in the same way. In the end, the analog/digtal rectifier and demodulator/modulator should be placed close together, since they share the common RF pins.

When implementing the floorplan (Fig. 4.7 (b)), it can be seen that the temperature sensor analog block is placed in the upper left corner, while the digital logic block is located in the lower right corner. The SC interface and the digi-

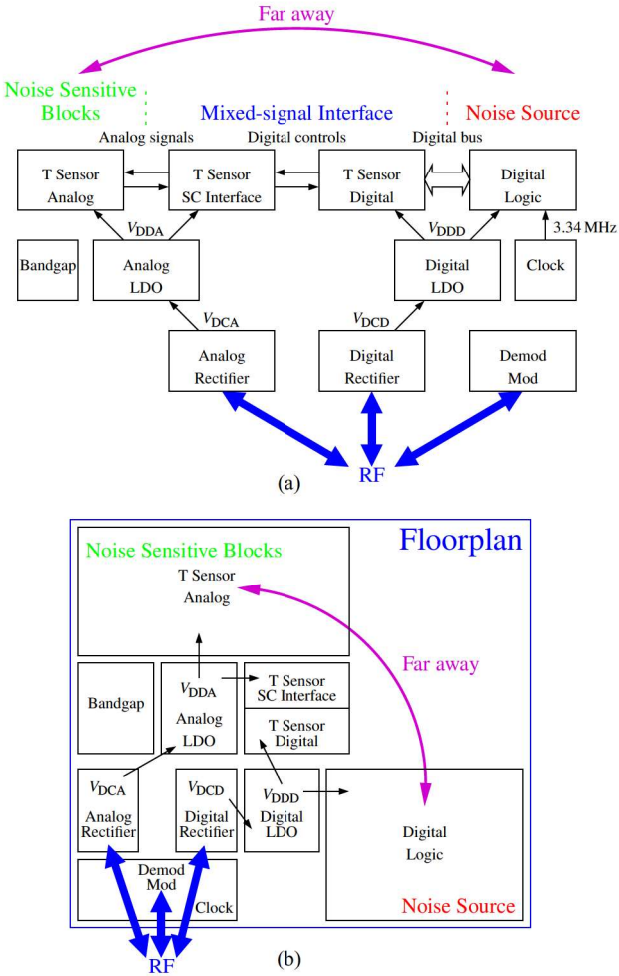


Fig. 4.7 (a) the concept of separation of noise insensitive and noise sensitive blocks and (b) the realization in this floorplan

tal block of the temperature sensor are located in the middle of the chip. The PMU is located on the left bottom, as the analog and digital power paths are

efficiently separated. At the end, all RF-related blocks connect to the lower left corner, where the RF pads are located.

4.4.2 Final layout

The final layout is shown in Fig. 4.8. The entire chip utilizes 22 pads, including RF pads, analog test pads and digital test pads. Only the two RF pads are mandatory for the chip functionality.

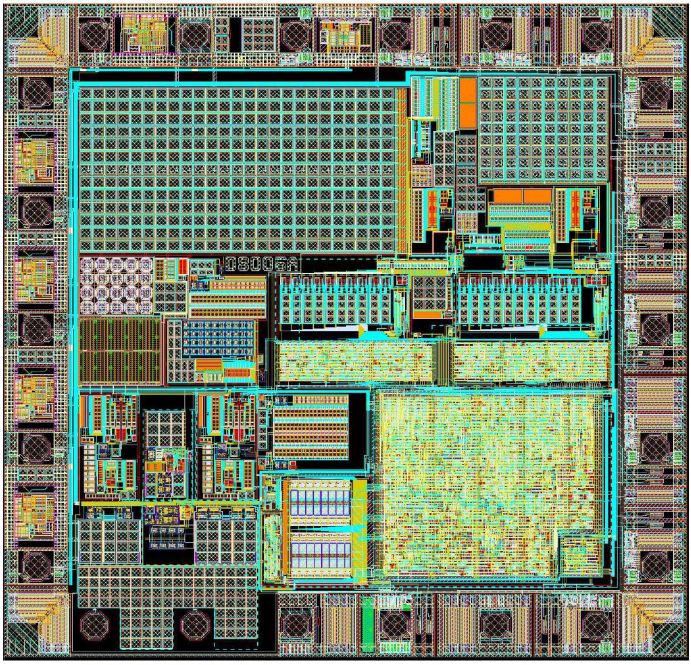


Fig. 4.8 The final layout of this proposed RFID temperature sensor

4.5 Summary

In this chapter, the system integration and physical design are presented. This chip utilizes ISO 14443 type B in the physical layer. The communication layer is significantly simplified by introducing only readout command and write commands. Since the temperature sensor is sensitive to the AC supply noise, a serial readout command is introduced to reduce the supply noise during the temperature sensing. The system integration is achieved by designing time-to-digital converter and digital control logic. Finally, the layout of the chip is optimized to reduce the noise coupling from the digital logic to the analog sensor. A dedicated floor plan ensures that analog and digital parts are separated as far as possible.

Chapter 5

Experimental results

5.1 Measurement setup

The RFID temperature sensor SoC [90, 89] has been implemented in a commercial 0.35-µm CMOS technology with four metal layers (Fig. 5.1). The entire chip occupies approximately 5.06 mm^2, including many test structures and test pads required only for measurement purposes. The RFID PMU, front end, temperature sensor, and digital logic use active areas of approximately 0.56 mm^2, 0.23 mm^2, 0.85 mm^2 and 0.5 mm^2, respectively.

In order to measure the RFID temperature sensor efficiently and precisely, the chip is mounted on a 1.4 mm aluminum core directly to achieve a minimum thermal resistance using chip-on-board (COB) technology (Fig. 5.2). The top 0.2 mm FR4 layer is milled open to expose the aluminum core, onto which the die is bonded by thermally conducting adhesive. Near the chip, a placeholder is reserved for a PT1000 reference temperature sensor. The four-wired PT1000 resistor also has good thermal contact to the aluminum core, so that the PT1000 shares the same temperature with the chip. Finally the chip is sealed with epoxy

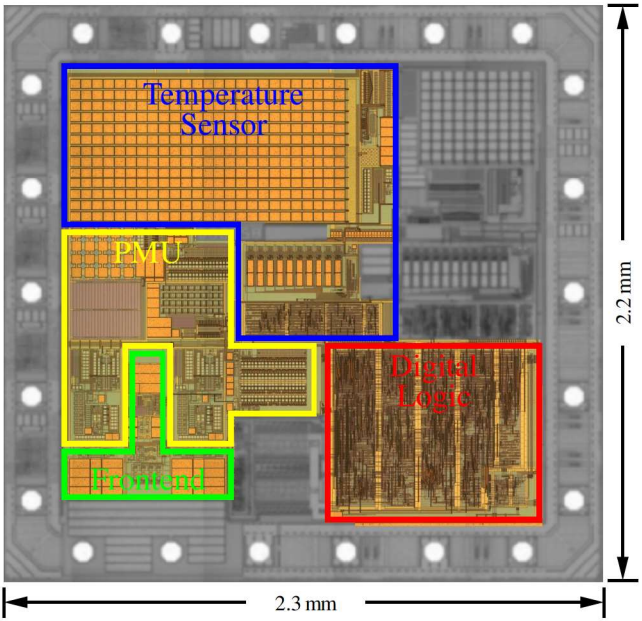
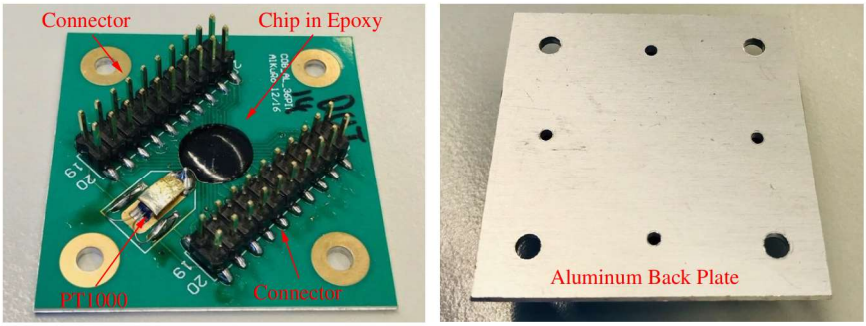


Fig. 5.1 Photograph of the test chip [90, 89]. The colored region are actively used, while the gray-shaded regions are used mainly for testing purposes.

resin. The signals from all pins are routed to a connector for measurement purposes.

The measurement setup for RFID communication and PMU characterization is shown in Fig. 5.3. An external coil and a tuning capacitance are attached for RFID communication because these are not implemented on chip. No further external components are required, which helps to minimize size and cost of the final assembly. A commercially available RFID reader module based on the TI TRF7970A interrogator IC [82] is used to communicate with the chip. The MCU on the reader module was programmed to detect the temperature sensor and control the readout process. The readout data was logged via a USB port for further signal processing. The PT1000 reference sensor was read out in parallel



(a) (b)

Fig. 5.2 (a) Chip-on-board assembly for the characterization of the SoC and (b) its aluminum back plate.

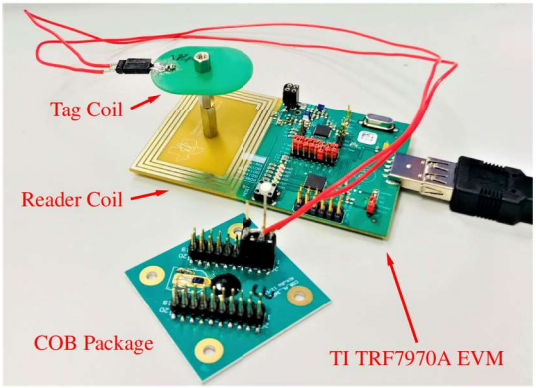
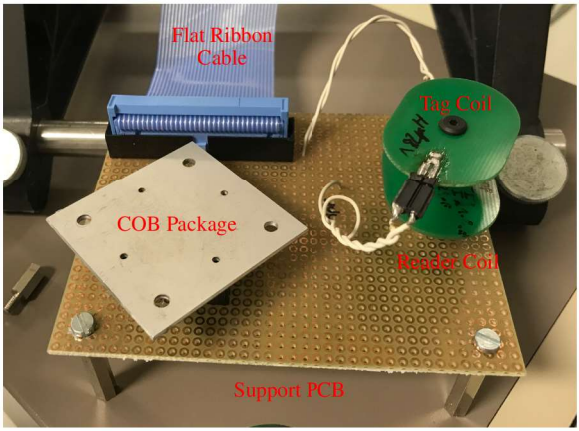


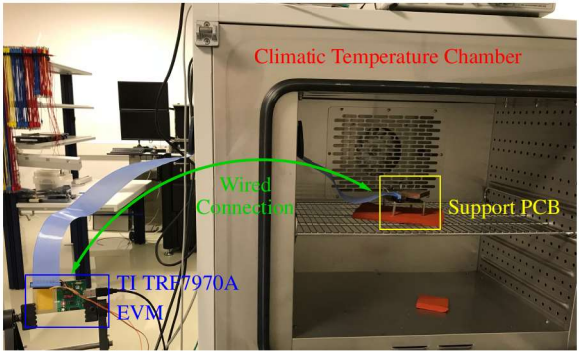
Fig. 5.3 Setup for the in-system characterization of the SoC. The wires between the SoC and the tag coil are not twisted minimize parasitic capacitance.

by the measurement setup while data was continuously received by the RFID reader.

For temperature sensor characterization, the measurement were performed with an additional PCB (Fig. 5.4 (a)) placed in a temperature chamber. The COB assembly is mounted on a board, which provides a solid mechanical and



(a)



(b)

Fig. 5.4 (a) The support PCB provides the mechanical stability and necessary connections. (b) Measurement in a climatic temperature chamber. The SoC and the reader coil are located in the chamber, while the interrogator is outside.

electrical connection to the tag coil and a stable RFID wireless connection to the custom reader coil. The COB assembly can be easily exchanged. The custom reader coil is connected to the reader outside the temperature chamber using a 50 Ω high temperature range flat ribbon cable (Fig. 5.4 (b)). The temperature of

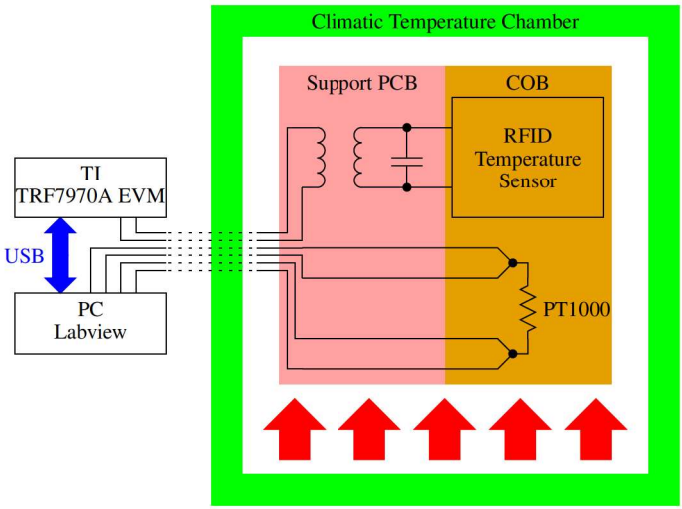


Fig. 5.5 Setup of the SoC measurement with climatic temperature chamber.

the chamber is configured as a ramp function from 0 °C to 125 °C in one hour. Data from the RFID temperature sensor and the PT1000 resistor were recorded simultaneously by a dedicated Labview program (Fig. 5.5).

5.2 RFID communication & PMU characterization

The communication and power supply measurements were performed at room temperature. To support the custom RFID command, the direct mode (transparent communication without the protocol handling defined in ISO/IEC 14443 type B [73]) of the TRF7970A interrogator was utilized. Fig. 5.6 (a) shows the command and response bit streams, which were sampled with an oscilloscope. First, the reader's RF signal is activated. Then, three commands are sent to the tag, namely: power up the sensor, start the sensor for measurement and perform sensor data readout. It can be seen that after the serial readout command, the tag starts to transmit the sensor data until the RF power is turned off. The DC

voltages V_{DCA} and V_{DCD} are measured as well. During operation V_{DCA} varies between approximately 2 V and 2.5 V, while V_{DCD} stays approximately 2.3 V. Fig. 5.6 (b) shows the details of the "sensor power on" command execution.

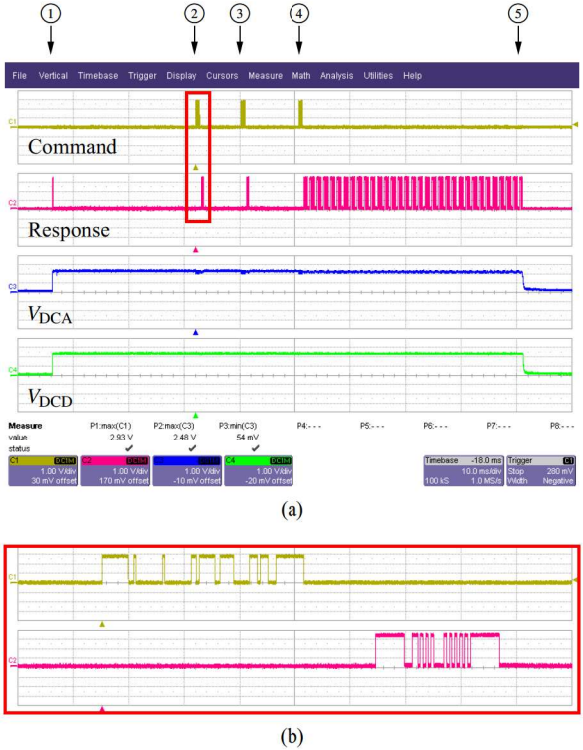


Fig. 5.6 (a) RFID command and response on the reader side and DC voltages on the tag side. The events are listed: ①: tag power on, ②: temperature sensor power on, ③: temperature sensor start, ④: temperature sensor data serial read-out, ⑤: tag power off. (b) Zoomed communication signals at sensor power on command

In Fig. 5.7 the on-chip communication signal and supply voltage on the tag side are shown. Before the command is given to the tag, the tag is in an idle

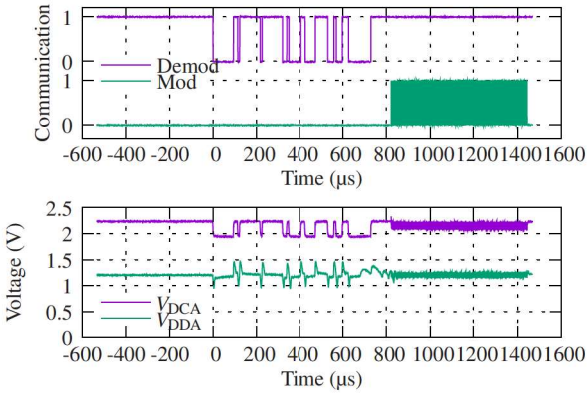


Fig. 5.7 Communication and power management voltages V_{DCA} and V_{DDA} on the tag side. The signals are shown in three ranges: ①: idle, ②: command, ③: response

phase. During the idle phase, the V_{DCA} and V_{DDA} have the minimal supply noise, which is smaller than 25 mV peak-to-peak amplitude. When the command is given, the V_{DCA} and V_{DDA} have the interference with the peak-to-peak amplitudes of 300 mV and 540 mV, respectively. During the response phase, the V_{DCA} and V_{DDA} have the interference with the peak-to-peak amplitude of 150 mV and 120 mV, respectively. It can be seen that the command generates a much higher interference amplitude than the response.

The sampling rate of the temperature sensor is approximately 1 kHz. The command has a 106 kHz or lower frequency band, while the response is located at 848 kHz, which is the subcarrier frequency. Thus the frequency of the interference from the command is closer to the temperature sensor sampling rate than the response. Thus the interference of RFID commands dominates the impact on the temperature sensor.

5.3 Wireless sensor characterization

The control sequence for the proposed RFID temperature sensor is shown in Fig. 5.8. First, the reader's RF signal is activated. Then, four commands are sent to the tag, namely: set the sensor PWM output to the digital test pin, power up the sensor, start the sensor for measurement and perform sensor data readout. It can be seen that the voltage of the test pin is switched to high, after setting the sensor PWM output to the digital test pin. Then after the sensor starts, the test pin starts to output the PWM signal, which can be checked for sensor performance as well. In the following measurements, the sensor output data, which are transmitted by RFID communication, are used as valid sensor data.

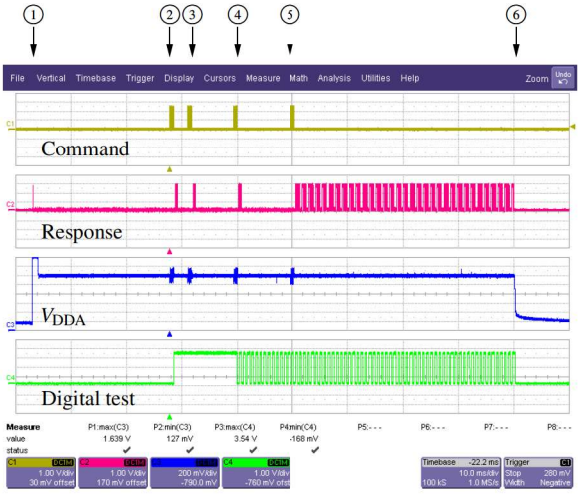


Fig. 5.8 (a) RFID command and response on the reader side and test signals on the tag side. The events are listed: ①: tag power on, ②: set sensor PWM output to the digital test pin, ③: temperature sensor power on, ④: temperature sensor start, ⑤: temperature sensor data serial readout, ⑥: tag power off.

5.3.1 Accuracy characterization

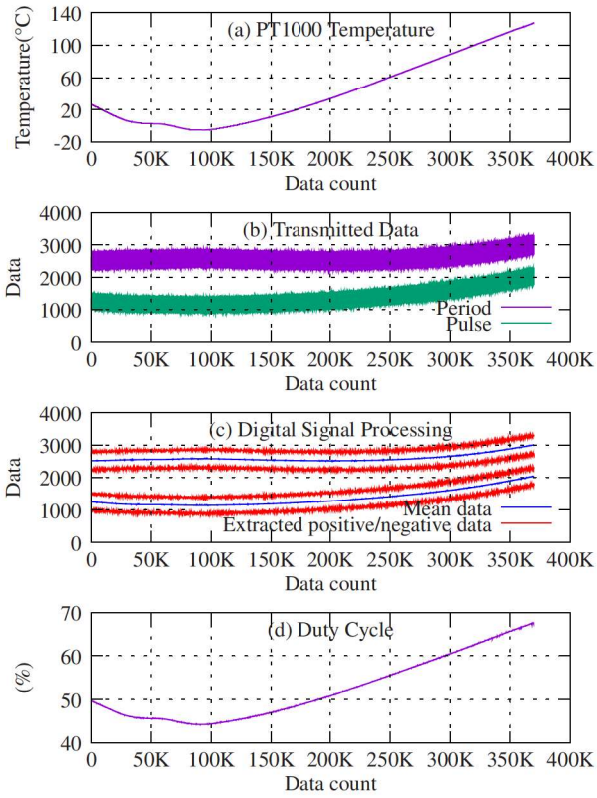


Fig. 5.9 The data processing from raw data to valid duty cycle. (a) the reference temperature, (b) raw period and pulse data, (c) the extracted data for mean value calculation, (d) the calculated duty cycle

In the climatic temperature chamber, the accuracy of this proposed RFID temperature sensor is characterized. In order to obtain sufficient measurement data to eliminate noise, the temperature slope in the chamber is set as low as possible, so that the entire temperature curve lasts approximately 3 hours. In

the meantime, the RFID reader continuously reads the sensor output via the serial readout command. Due to the RAM limitation of the reader MCU, only a hundred data are stored before the reader switches off the field. The data is processed and sent to the customized Labview program on the PC, so that the data can be stored on the hard drive. At the same time, PT1000 is also continuously being readout, and reference temperatures can be recorded.

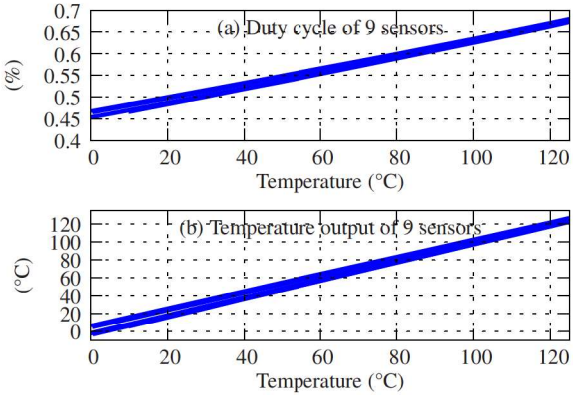


Fig. 5.10 (a) The duty cycle and (b) temperature output from nine samples before calibration

In Fig. 5.9 (a), the total amount data is approximately 370 thousand. At the beginning, the temperature falls from room temperature to slightly below 0 °C slowly. Then the chamber increases the temperature to approximately 130 °C, so that the range 0 °C to 125 °C is covered. In Fig. 5.9 (b), the raw data "Period" and "Pulse" extracted directly from RF communication are plotted. It can be seen that due to the sensor functionality, which generates positive and negative data, each data varies in a wide range, so that the offset can be compensated. Furthermore, the data is processed in a digital signal processing (DSP) unit, which is implemented as a "Matlab" [72] program on the PC. The raw data are filtered and separated for positive and negative data in Fig. 5.9 (c). The

mean values are calculated and averaged with a large amount of continuous data. The more data averages, the less noise remains in the value. An the end, the duty cycle is calculated from the mean period data and the mean pulse data (Fig. 5.9 (d)).

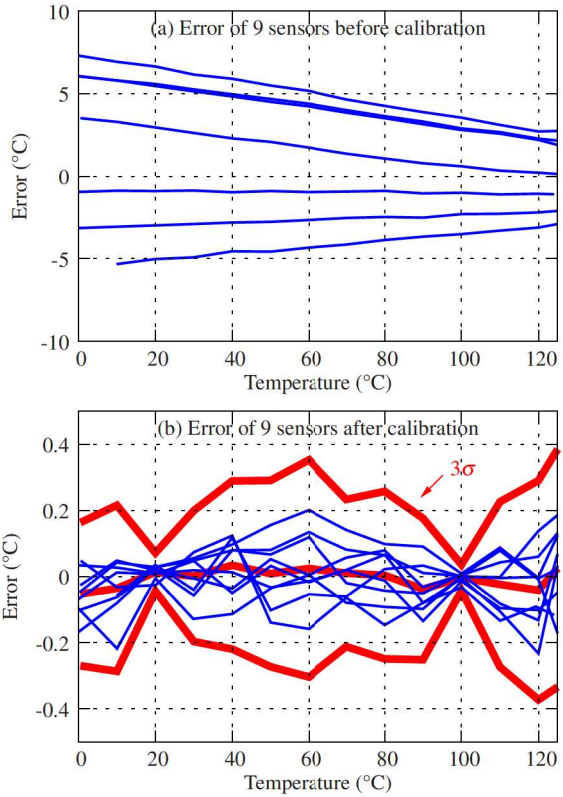


Fig. 5.11 Measured temperature error of 9 sensors (a) before and (b) after two-point calibration at 20 °C and 100 °C; thick red lines indicate the mean values and the $\pm 3\sigma$ limits.

Nine samples were used to perform a statistical measurement with the same digital signal processing. The duty cycles of the nine samples are shown in Fig. 5.10 (a), while the nine outputted temperature are shown in Fig. 5.10 (b). Good linearity means that most of the residual error can be eliminated by a two-point calibration.

The temperature error referred to the PT1000 temperature before calibration is shown in Fig.5.11 (a). The errors of 9 samples caused by process variation are distributed over a range of ±8 °C. Since the errors depend almost linearly on the temperature, they can be compensated by a two-point calibration at 20 °C and 100 °C. In Fig. 5.11 (b), the error interval is reduced to ±0.2 °C. The 3σ error is calculated to be in a range of ±0.4 °C from 0 °C to 125 °C.

5.3.2 Noise characterization

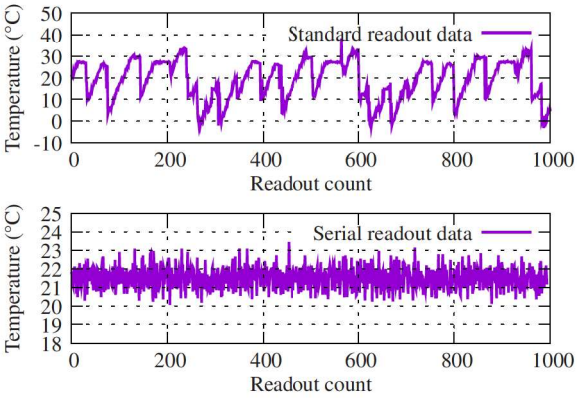


Fig. 5.12 Temperature data acquired with standard readout (upper graph) and serial readout (lower graph).

At room temperature, to verify the comparison of the standard readout command and the serial readout command with measurements, the time delay between temperature sensor start command (Fig. 5.8 ④) and the temperature sen-

sor readout command (Fig. 5.8 ⑤) is swept. The delay was slowly increased and the readout data was recorded for a long time duration so that statistical information could be derived. Finally, the recorded data is used to calculate the resolution for both cases, standard readout and serial readout.

Fig. 5.12 shows a small segment of the record. Both diagrams show 1000 data points each recorded at room temperature. The measured temperature for standard readout varies from −3.2 °C to 38.4 °C. For serial readout the range of the measurement results is reduced to 20 °C to 23.4 °C. The response for standard readout shows a more deterministic, periodic-like behavior, while serial readout seems to be more random. This indicates that the standard readout response is dominated by the supply interference, which is synchronized to the command. The serial readout response, on the other hand, avoids distorted data and displays the corresponding sensor noise itself. In summary, the RFID temperature sensor SoC achieves an uncalibrated resolution of 9.01 °C when using the standard readout, while serial readout achieves a resolution of 0.56 °C, see Table 5.1. serial readout improves the resolution by a factor of about 16.

Table 5.1 Summary of achieved resolution (uncalibrated)

Command	Resolution (°C)	Dominant error source
Standard readout	9.01	Supply interference
Serial readout	0.56	Sensor noise

5.4 Performance comparison with state-of-the-art RFID temperature sensors

A summary and a comparison of the performances is given in Table 5.2.

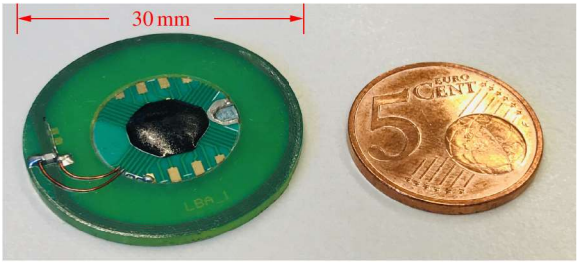
Table 5.2 Performance Summary and Comparison

Parameter	[36]	[43]	[44]	**This work[90, 89]**
CMOS process	0.13 µm	0.18 µm	0.18 µm	**0.35 µm**
Tag type	Passive	Passive	Passive	**Passive**
Frequency range	2.4 GHz	860 MHz ... 960 MHz	860 MHz ... 960 MHz	**13.56 MHz**
Temp. Sensor type	On-chip	On-chip	On-chip	**On-chip**
Temp. range	27 °C ... 45 °C	−20 °C ... 30 °C	−20 °C ... 50 °C	**0 °C ... 125 °C**
Inaccuracy	±0.4 °C[(2)] within 1 sample	±0.8 °C[(1)] within 9 samples	−1 °C/0.8 °C[(2)] within 3 samples	**±0.4 °C[(1)] within 9 samples**
Sensor power consumption	N/A	1.5 µW	13.2 µW	**3.5 µW**
Conversion time	N/A	40 ms	6 ms	**1.48 ms**
Energy per conversion	N/A	60 nJ	79.2 nJ	**5.18 nJ**
Calibration points	2	1	1	**2**

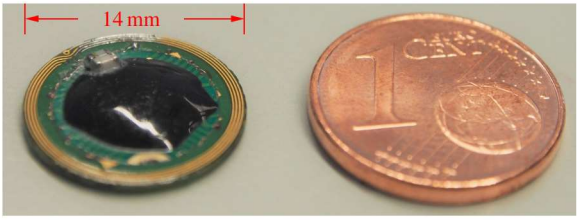
(1) 3σ inaccuracy
(2) Min, max inaccuracy

5.5 Demonstrator

The chip is finally assembled to demonstrator tags (Fig. 5.13 (a) (b)), which consists of a 14 mm (Fig. 5.13 (a)) and 30 mm (Fig. 5.13 (b)) diameter coil and a tuning capacitance. Due to the reuse of the COB shown in Fig. 5.2, the demonstrator also contains an aluminum back plate, which attenuates the received energy compared to the measurement assembly shown in Fig. 5.3. The demonstrator is then covered by a water-proof coating, so that it can be put into a liquid to measure its temperature wirelessly (Fig. 5.14).



(a)



(b)

Fig. 5.13 RFID transponder with (a) 14 mm and (b) 30 mm diameter coil

The results, which are directly processed and illustrated in a LabView [74] program (Fig. 5.14), indicate that the demonstrator runs as expected and allows to monitor temperature conditions continuously.

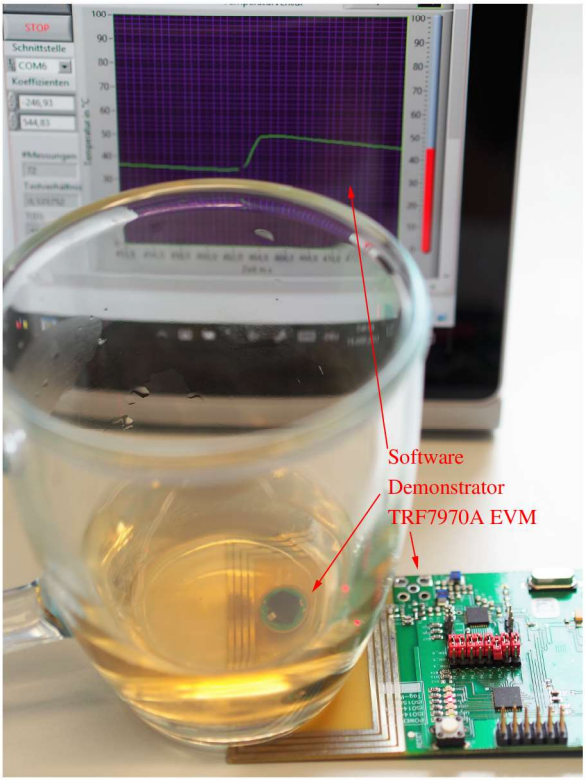


Fig. 5.14 Demonstrator setup for water temperature measurement with demonstrator software

Chapter 6

Summary and outlook

This dissertation presents the design methodology and implementation of fully passive RFID temperature sensor SoC. The proposed wireless SoC chip achieves an accuracy of ±0.4 °C (3σ) from 0 °C to 125 °C with 676 Samples/s.

The low-power high-accuracy temperature sensing is provided by a dedicated time-domain topology. Compared to the traditional voltage-domain topology, this topology achieves a similar operational range and sensor accuracy while significantly reducing design complexity and enabling a more potential low-power design strategy. The model of this topology is built and verified to explain its functionality. The challenges of transistor-level design, including the non-idealities of the switches, the propagation delay of the comparator and the offset voltage of the comparator are solved by implementing different design techniques. The experimental results show that the accuracy of the temperature sensor reaches −0.1 °C to 0.5 °C in the entire temperature range from −40 °C to 125 °C and ±0.1 °C in the range from 0 °C to 125 °C, while the resolution is 0.3 °C.

The fully passive RFID communication is provided by RFID PMU and RFID frontend. The implementation consists of rectifier, bandgap, LDO, lim-

iter, demodulator, modulator and clock recovery. The simulation results show that the functional blocks operate successfully as expected.

This thesis presents the supply noise analysis as an essential contribution of the design methodology, since high accuracy of this wireless sensor is required. In order to efficiently analyze the supply noise, the noise path is divided into three crucial processes: noise generation, noise amplification and noise digitization. The supply noise is generated from different sources, e.g. carrier frequency, RFID communication, load condition and geometry, so that it occupies a wide frequency spectrum. Then the supply noise is amplified by the PMU, which includes bandgap reference and LDO. To analyze the frequency response of the gain (PSR), the typical models of bandgap reference and LDO are built. The PSR simulation shows that the typical PMU amplifies the supply interference in the RFID communication frequency band. This amplified supply noise will affect the performance of the temperature sensor. To compare the performance of this proposed temperature sensor, two other state-of-the-art time-domain temperature sensors are modeled. In DC analysis, the model of this proposed temperature sensor reaches 0.0006 °C/mV, which is lowest among the three topologies. In AC analysis, the proposed temperature sensor outputs more noise, as the frequency of supply noise increases. Since the temperature sensor is sensitive to the AC supply noise, a serial readout command in system integration is introduced to reduce the supply noise during the temperature sensing.

The entire SoC is designed and layouted in a commercial 0.35-µm CMOS technology. The chip is packaged with COB technology and characterized for RFID communication and sensor performance. During RFID communication, the supply ripple is measured with a maximum 540 mV peak-to-peak amplitude. If the sensor operates under this condition, the sensor has a resolution of 9.01 °C. With the serial readout command, the sensor operates with a cleaner supply voltage so that the sensor achieves a resolution of 0.56 °C. The serial readout command improves the sensor resolution by a factor of approximately 16. The inaccuracy of the wireless temperature sensing is achieved with ±0.4 °C (3σ)

from 0 °C to 125 °C. At the end, the demonstrator is built to demonstrate a potential wireless environmental monitoring application with only one off-chip antenna and one resonance cap.

The research presented in this dissertation has opened a number of research lines that should be explored in the future.

The PSR of the PMU can be further improved. In this dissertation, the modeling of the bandgap and LDO is explored. The models show that a full-spectrum PSR can be realized with proper design. A full-spectrum PSR will significantly reduce the ripple, which occurs in a wide frequency range. A noise-free supply can enable the maximum performance of the integrated sensor. The full-spectrum PSR is useful for several applications, not only the RFID sensors, but also the Wheatstone bridge interface and the voltage-controlled oscillator (VCO). Four resistors are utilized by wheatstone bridge [42], which is highly affected by the supply voltage variations. The balanced bridge has perfect rejection of the supply noise, but in practice the unbalanced bridge suffers from noise due to finite PSR. The low supply sensitivity of the VCO is one of the challenges in PLL design. Some state-of-the-art designs [6] utilize additional regulators to stabilize the control voltage, while they generates additional energy waste and voltage headroom problems.

On the other hand, sensors can be made more immune to supply noise. The analog sensors consist of many basic blocks, e.g. differential pairs, current mirrors, switched-capacitor circuits and so on. They have different PSR characteristics and influence of the supply noise, so that the bottleneck of the system can be defined by one or two particular power paths. The new design methodology can be developed so that these bottlenecks can be automatically analyzed, verified and optimized. Thus, the analog sensors become stronger that they can be implemented in more application scenarios.

From the application's perspective, the entire system can be redesigned and optimized with more communication distance, more robustness and lower cost. The HF RFID has a natural communication distance up to 10 cm, while UHF RFID [64, 77] enables the communication range to several meters. With the

combination of sensors, we can from longer distance not only identify the object but also sense the status of the object. This significantly expands application scenarios such as supply chain & logistics, retail, health care and industrial manufacturing. Of course, the sensor functionality must be highly robust and cost effective to make the tags affordable in mass production. There are several ways to increase robustness and reduce costs. The sensor can be improved to achieve better initial accuracy so that only one-point trimming or no trimming is needed. Development costs can be reduced by using an external sensor communication interface so that the tag chip can easily be utilized with different external sensors for different applications. CMOS production costs can be reduced by reducing the active chip area, reducing the number of pins and utilizing smaller process nodes.

I believe in a wireless future [66], a future where everything intuitively connects. This belief drove the design of our wireless sensors forward. They have been made possible with the development of this proposed RFID sensor SoC chip. It achieves best-in-class performance to produce intelligent, high accurate and high efficient temperature sensing, while delivering a consistent RFID connection. We're just at the beginning of a truly wireless future we've been working towards for many years, where technology enables a seamless and automatic connection between everything.

Chapter 7

Zusammenfassung und Ausblick

Diese Dissertation stellt die Entwurfsmethodik und die Implementierung von vollständig passiven RFID Temperatursensoren SoC vor. Der vorgeschlagene drahtlose SoC Chip erreicht eine Genauigkeit von ±0.4 °C (3σ) von 0 °C zu 125 °C mit 676 Samples/s.

Die hochpräzise Temperaturmessung mit niedriger Leistung wird durch eine spezielle Zeitdomainstopologie bereitgestellt. Im Vergleich zur traditionellen Spannungdomainstopologie erreicht diese Topologie eine ähnliche Reichweite und Sensorgenauigkeit bei gleichzeitiger signifikanter Reduzierung der Design Komplexität und ermöglicht eine potentiellere Low-Power Designstrategie. Das Modell dieser Topologie wird gebaut und verifiziert, um ihre Funktionalität zu erklären. Die Herausforderungen des Transistor-Level Designs, einschließlich der Nicht-Idealitäten der Schalter, der Laufzeitverzögerung des Komparators und der Offsetspannung des Komparators, werden durch die Implementierung verschiedener Designtechniken gelöst. Die experimentellen Ergebnisse zeigen, dass die Genauigkeit des Temperatursensors –0.1 °C bis 0.5 °C im gesamten

Temperaturbereich von –40 °C bis 125 °C und ±0.1 °C im Bereich von 0 °C bis 125 °C, während die Auflösung 0.3 °C ist.

Die vollständig passive RFID Kommunikation wird durch RFID PMU und RFID Frontend bereitgestellt. Die Implementierung besteht aus Gleichrichter, Bandgao, LDO, Limiter, Demodulator, Modulator und Taktrückgewinnung. Die Simulationsergebnisse zeigen, dass die Funktionsblöcke wie erwartet erfolgreich arbeiten.

Diese Arbeit stellt die Analyse des Versorgungsrauschens als einen wesentlichen Beitrag der Entwurfsmethodik dar, da eine hohe Genauigkeit dieses drahtlosen Sensors erforderlich ist. Um das Versorgungsrauschen effizient zu analysieren, wird das Rausch in drei entscheidende Prozesse unterteilt: Rauscherzeugung, Rauschverstärkung und Rauschdigitalisierung. Das Versorgungsrauschen wird aus verschiedenen Quellen erzeugt, z.B. Trägerfrequenz, RFID Kommunikation, Lastzustand und Geometrie, so dass es ein breites Frequenzspektrum einnimmt. Dann wird das Versorgungsrauschen durch das PMU verstärkt, das eine Badngap Referenz und LDO beinhaltet. Um den Frequenzgang der Verstärkung (PSR) zu analysieren, werden die typischen Modelle von Bandgap Referenz und LDO erstellt. Die PSR Simulation zeigt, dass die typische PMU die Versorgungsstörung im RFID Kommunikationsfrequenzband verstärkt. Dieses verstärkte Versorgungsrauschen beeinträchtigt die Genauigkeit des Temperatursensors. Um die Genauigkeit dieses vorgeschlagenen Temperatursensors zu vergleichen, werden zwei weitere moderne Zeitdomain Temperatursensoren modelliert. In der DC Analyse erreicht das Modell dieses vorgeschlagenen Temperatursensors 0.0006 °C/mV, was unter den drei Topologien am niedrigsten ist. In der AC Analyse gibt der vorgeschlagene Temperatursensor mehr Rauschen aus, wenn die Frequenz des Versorgungsrauschens zunimmt. Da der Temperatursensor empfindlich auf das Wechselstromversorgungsrauschen reagiert, wird ein serieller Auslesekommando in der Systemintegration eingeführt, um das Versorgungsrauschen während der Temperaturmessung zu reduzieren.

Der gesamte SoC ist in einem kommerziellen 0.35-µm CMOS Technologie entworfen. Der Chip ist mit der COB Technologie verpackt und durch

RFID Kommunikation und Sensor Performance ausgemessen. Während der RFID Kommunikation wird die Versorgungsspitze mit einer maximalen Amplitude von 540 mV gemessen. Wenn der Sensor unter dieser Bedingung arbeitet, hat der Sensor eine Auflösung von 9.01 °C. Mit dem seriellen Auslesekommando arbeitet der Sensor mit einer saubereren Versorgungsspannung, so dass der Sensor eine Auflösung von 0.56 °C erreicht. Der serielle Auslesekommando verbessert die Sensorauflösung um den Faktor 16. Die Ungenauigkeit der drahtlosen Temperaturmessung wird mit ±0.4 °C erreicht. (3σ) von 0 °C bis 125 °C. Am Ende wird der Demonstrator gebaut, um eine mögliche drahtlose Umweltüberwachungsanwendung mit nur einer Off-Chip Antenne und einer Resonanzkapazität zu demonstrieren.

Die Forschung dieser Dissertation hat eine Reihe von Forschungslinien, die in der Zukunft untersucht werden sollten.

Das PSR des PMU kann weiter verbessert werden. In dieser Dissertation wird die Modellierung der Bandgap Referenz und des LDO untersucht. Die Modelle zeigen, dass ein Vollspektrum PSR bei richtigem Design realisiert werden kann. Ein Vollspektrum PSR reduziert die Welligkeit, die in einem breiten Frequenzbereich auftritt, deutlich. Eine rauschfreie Versorgung kann die maximale Performance des integrierten Sensors ermöglichen. Das Vollspektrum PSR eignet sich für mehrere Anwendungen, nicht nur für die RFID Sensoren, sondern auch für die Wheatstone Bridge Schnittstelle und den spannungsgesteuerten Oszillator (VCO). Vier Widerstände werden von Wheatstone Bridge [42] verwendet, die stark von den Schwankungen der Versorgungsspannung beeinflusst wird. Die symmetrische Brücke hat eine perfekte Unterdrückung des Versorgungsrauschens, aber in der Praxis leidet die unsymmetrische Brücke aufgrund von endlichem PSR unter Störungen. Die geringe Versorgungs- empfindlichkeit des VCO ist eine der Herausforderungen beim PLL Design. Einige moderne Designs [6] verwenden zusätzliche Regler, um die Steuerspannung zu stabilisieren, während sie zusätzliche Energieverschwendung erzeugen.

Auf der anderen Seite können Sensoren immuner gegen Versorgungsrauschen gemacht werden. Die analogen Sensoren bestehen aus vielen Grundkonstruktionen, z.B. Differentialpaaren, Stromspiegeln, SC Schaltungen usw. Sie haben unterschiedliche PSR Eigenschaften und Einfluss des Versorgungsrauschens, so dass die Schwäche des Systems durch ein oder zwei bestimmte Leistungspfade definiert werden kann. Die neue Entwurfsmethodik kann so entwickelt werden, dass diese Schwäche automatisch analysiert, verifiziert und optimiert werden können. Dadurch werden die analogen Sensoren stärker, so dass sie in weiteren Anwendungsszenarien eingesetzt werden können.

Aus Anwendungssicht kann das gesamte System mit mehr Kommunikationsreichweite, mehr Robustheit und niedrigeren Kosten neu entworfen und optimiert werden. Der HF RFID hat eine natürliche Kommunikationsreichweite von bis zu 10 cm, während UHF RFID [64, 77] die Kommunikationsreichweite auf mehrere Meter erhöht. Mit der Kombination von Sensoren können wir aus größerer Entfernung nicht nur das Objekt identifizieren, sondern auch den Status des Objekts erfassen. Damit werden Anwendungsszenarien wie Supply Chain & Logistik, Handel, Gesundheitswesen und industrielle Fertigung deutlich erweitert. Natürlich muss der Sensor sehr robust und kostengünstig sein, um die Tags in der Massenproduktion bezahlbar zu machen. Es gibt mehrere Möglichkeiten, die Robustheit zu erhöhen und die Kosten zu senken. Der Sensor kann verbessert werden, um eine bessere Initialgenauigkeit zu erreichen, so dass nur ein Punkt Trimming oder kein Trimming erforderlich ist. Durch die Verwendung einer externen Sensor Kommunikationsschnittstelle können die Entwicklungskosten reduziert werden, so dass der Tag Chip problemlos mit verschiedenen externen Sensoren für verschiedene Anwendungen eingesetzt werden kann. CMOS Produktionskosten können durch die Reduzierung der aktiven Chipfläche, die Reduzierung der Anzahl der Pins und die Nutzung kleinerer Prozessknoten reduziert werden.

Ich glaube an eine drahtlose Zukunft [66], eine Zukunft, in der alles intuitiv verbunden ist. Dieser Glaube hat das Design unserer drahtlosen Sensoren vorangetrieben. Sie wurden durch die Entwicklung dieses vorgeschlagenen

RFID Sensor SoC Chips ermöglicht. Es erreicht Spitz Performance bei der intelligenten, hochpräzisen und hocheffizienten Temperaturmessung und liefert gleichzeitig eine konsistente RFID Verbindung. Wir stehen erst am Anfang einer wirklich drahtlosen Zukunft, auf die wir seit vielen Jahren hinarbeiten, wo die Technologie eine nahtlose und automatische Verbindung zwischen allem ermöglicht.

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Abbreviations

AC Alternating current

ADC Analog-to-digital converter

ALU Arithmetic-logic unit

ASIC Application-specific integrated circuit

ASK Amplitude shift keying

BJT Bipolar junction transistor

BW Band width

CM Clock management

CMOS Complementary metal-oxide-semiconductor

COB Chip on board

CPU Central processing unit

CTAT Complementary to absolute temperature

DC Direct current

DSP Digital signal processing

EOF End of frame

ETU Elementary time unit

HF High frequency

ID Identification

IoT Internet of things

LDO Low dropout regulator

MCU Micro-controller unit

MTP Microtiter plate

pbb Pipe-based bioreactor

PCB Printed circuit board

PLL Phase locked loop

PMU Powe management unit

POR Power on rest

PSR Power supply rejection

PTAT Proportional to absolute temperature

PVT Process voltage temperature

PWM Pulse width modulation

RAM Random access memory

RF Radio frequency

RFID Radio frequency identification

SAR Successive approximation register

SC Switched capacitor

SoC System on chip

SOF Start of frame

SPI Serial peripheral interface

TC Temperature coefficient

TDC Time-to-digital converter

UHF Ultra high frequency

ULP Ultra low power

USB Universal serial bus

VCO Voltage controlled oscillator

VLSI Very large scale integration

WSN Wireless sensor network