Enabling control of matter at the atomic level: Atomic Layer Deposition and Fluorocarbon-based Atomic Layer etching

Dissertation

by

Stefano Dallorto

A dissertation submitted in partial fulfillment of
the requirements for the degree of

Doctor of Philosophy
(Dr. Ing.)

Dept. of Microelectronic and Nanoelectronic Systems,
Ilmenau University of Technology

Date of submission: 10.09.2019
Date of defense: 18.12.2019
URN: urn:nbn:de:gbv:ilm1-2019000480

Supervisor	Prof. Dr. -Ing. habil. Ivo W. Rangelow
First reviewer	Dr. Adam Schwartzberg
Second reviewer	Univ. -Prof. Dr. -Ing. Steffen Strehle

This work has been supported by Oxford Instruments Plasma Technology, which I warmly thank for giving me the opportunity of pursuing my doctoral studies.

Work at the Molecular Foundry was supported by the Office of Science, Office of Basic Energy Sciences, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

Declaration

I certify that I prepared the submitted thesis independently without undue assistance of a third party and without the use of others than the indicated aids. Data and concepts directly or indirectly taken over from other sources have been marked stating the sources.

Further persons were not involved in the content-material-related preparation of the thesis submitted. In particular, I have not used the assistance against payment offered by consultancies or placing services (doctoral consultants or other persons). I did not pay any money to persons directly or indirectly for work or services which are related to the content of the thesis submitted.

So far the thesis has not been submitted identically or similarly to an examination office in Germany or abroad. I have been notified that any incorrectness in the submitted above mentioned declaration is assessed as attempt to deceive and, according to § 7 para. 10 of the PhD regulations, this leads to a discontinuation of the doctoral procedure.

Berkeley, September 10, 2019 Stefano Dallorto

To O. G.

Abstract

The diminishing size of devices has necessitated the development of new patterning, deposition and etch techniques at ever-finer resolution, now approaching the atomic scale. Current trends in device manufacturing impose stringent requirements on nanoscale processing techniques, in terms of material properties and dimensional control. At the required nanoscale dimensions, additionally, surface composition and damage will be as important as physical dimensions for the desired functionality. Ultimately, the deposition and removal of arbitrary materials with single atomic layer precision are required. In this work I will present the insights of my work into fabrication processes and characterization techniques needed in the era of controlling matter at the atomic level using atomic layer deposition (ALD) and atomic layer etching (ALE).

To address the challenges in atomic scale manufacturing, a solid understanding of materials and their physical and chemical interactions is required. In this work, the synergy between materials and different fabrication processes is investigated. By studying how ALD performs on spacer defined double patterning (SDDP) I demonstrate the engineering of sub-10 nm features. SDDP is generally limited in resolution due to lack of nanoscale processes at sub-10 nm dimensions. Here, I establish how thermal ALD allows for conformal deposition of a titanium dioxide spacer layer without damaging or modifying any substrate. In conclusion, the first successful fabrication of 7.5 nm titanium oxide features using SDDP is made possible by atomic scaled processes.

While ALD has become productive enough to become a mainstream technology, the etch counterpart ALE has been more challenging. Indeed, removing material one atomic layer at a time is a complex scientific problem, especially when directional etching is required. In my work, a major goal was to develop methodologies that would allow the use of existing plasma etching tools for ALE. In this context, this work establishes and evaluates a cyclic fluorocarbon (FC) based approach for ALE of silicon dioxide, characterizes the mechanisms involved, and evaluates the impact of processing parameters. Using a cyclical FC and argon plasma process it is possible to atomically etch silicon oxide in a conventional plasma etch tool with minimal modifications. Plasma-based ALE allows for the directional etching required for deep narrow structures. For the first time, using the FC-based ALE processes, aspect ratio independent etching and high fidelity

pattern transfer have been achieved. This result is obtained through a detailed study of the impact of plasma parameters on the SiO_2 etch performance and using this information to achieve self-limiting behavior.

Overall, this work proves how new technology nodes are enabled by ALD and ALE as part of the increasing trend toward the atomic scale processing.

Zusammenfassung

Die fortschreitende Miniaturisierung von Halbleiterschaltkreisen erfordert die Entwicklung neuartiger Strukturierungs-, Abscheidungs- und Ätzmethoden. Die dafür erforderliche Auflösung nähert sich heutzutage atomaren Maßstäben. Die derzeitigen Trends in der Fabrikation von elektronischen Schaltkreisen stellen strenge Anforderungen an die verwendeten Nanostrukturierungsmethoden, in Bezug auf Kontrolle der Materialeigenschaften und der Strukturabmessungen. Für diese nanoskalige Strukturen sind außerdem Oberflächenzusammensetzung und Oberflächendefekte genauso wichtig wie die Strukturabmessungen, um die gewünschte Funktionalität zu erreichen. Letztendlich ist es daher notwendig beliebige Materialien mit der Präzision einzelner atomarer Lagen abzuscheiden und abzutragen. Die vorliegende Arbeit untersucht geeignete Fabrikations- und Charakterisierungsprozesse für die Ära der atomar genauen Materialstrukturierung mittels sogenannter Atomic Layer Deposition (ALD) und Atomic Layer Etching (ALE).

Um die Herausforderungen atomar genauer Materialstrukturierung zu adressieren ist ein tiefgehendes Verständnis der Materialien und ihrer physikalisch-chemischen Wechselwirkungen von Nöten. In der vorliegenden Arbeit wird die Synergie verschiedener Materialien und Fabrikationsprozesse untersucht. Durch Anwendung von ALD für die Doppelstrukturierung mittels Spacer-Technik (spacer defined double patterning, SDDP) wird gezeigt wie sich Strukturen mit Dimensionen unterhalb von 10 nm herstellen lassen. Generell ist die Auflösung von SDDP durch das Fehlen geeigneter Nanofabrikationsprozesse für Strukturen unterhalb von 10 nm limitiert. Die Arbeit etabliert, dass thermische ALD eine konforme Abscheidung einer Titandioxid-Spacer-Schicht erlaubt, ohne dabei das darunterliegende Substrate zu beschädigen oder zu modifizieren. Zusammenfassen lässt sich sagen, dass die erste erfolgreiche Fabrikation von 7.5 nm breiten Titanoxidstrukturen mittels SDDP nur durch die Anwendung von Prozessen auf atomarem Maßstab ermöglicht wurde.

Während ALD bereits zu einer produktiven Standardtechnologie geworden ist, erweist sich die Etablierung des korrespondieren Ätzprozesses, nämlich ALE, als ungleich schwieriger. Tatsächlich ist die kontrollierte Materialabtragung um jeweils eine Atomlage ein komplexes wissenschaftliches Problem. Dies gilt besonders für direktionales Ätzen. Ein

Hauptziel der Arbeit besteht in der Entwicklung von Methoden, die es erlauben existierende Plasmaätzanlagen für ALE zu verwenden. In diesem Zusammenhand etabliert und evaluiert diese Arbeit einen zyklischen Prozess basierend auf Fluorcarbonen (FC) für ALE von Siliziumdioxid. Es werden die beteiligten Reaktionsmechanismen charakterisiert und der Einfluss der Prozessparameter evaluiert. Mittels eines zyklischen FC- und Argon-Plasmas ist es möglich Siliciumdioxid atomar genau in einer minimal modifizierten, konventionellen Plasmaätzanlage zu ätzen. Plasma-basiertes ALE erlaubt direktionales Ätzen, das für tiefe, schmale Strukturen erforderlich ist. Zum ersten Mal werden hier sowohl seitenverhältnisunabhängiges Ätzen als auch hohe Zuverlässigkeit beim Strukturtransfer mittels FC-basiertem ALE erreicht. Das Resultat wird durch eine detaillierte Untersuchung des Einflusses der Plasmaparameter auf das Ätzverhalten von Siliziumdioxid und Anwendung der gewonnen Informationen auf ein selbstlimitierendes Verhalten ermöglicht.

Zusammengefasst demonstriert die vorliegende Arbeit wie neue Technologieknoten, die Teil des zunehmenden Trends zu atomar genauer Halbleiterprozessierung sind, durch ALD und ALE ermöglicht werden.

Contents

Chapter 1

Introduction

Overview

The goal of this introductory chapter is to give a scientific framework and motivation for this dissertation. Given current challenges in the manufacturing world, it has become necessary to develop new techniques that allow atomic scale control of matter. Layer-by-layer fabrication techniques have been identified as an answer to the sub-10 nm fabrication demand. Atomic layer deposition (ALD) and atomic layer etching (ALE) will be introduced as the techniques able to add and remove materials with the required level of control. The development of these new processes is highly interdisciplinary, requiring expertise from multiple fields including chemistry, physics, and nanofabrication science. This was achieved through collaborative research between world-class, interdisciplinary experts in academia and industry. This joint research effort, led by me, produced advanced materials, processes, and characterization techniques through a variety of cutting-edge techniques either developed for this work or pushed to their experimental limits. This chapter ends with a detailed overview of this dissertation, helping the reader envision the full work.

1.1 Advanced technology nodes

Advanced manufacturing requires precise control during nanofabrication pattern transfer in order to further shrink critical dimensions (CD). Current manufacturing is characterized by the need to mass produce features that have 10 nm CD and require CD variation of 0.5 nm or less.[1-3] In addition to pattern transfer fidelity in photolithography,

advanced semiconductor device fabrication increasingly demands atomistic surface engineering.[4, 5] Following the trajectory of Moore's law, integrated circuit devices are shrinking every year, and their structures have become more complex.[6-10] In the next ten years, acceptable feature size variability will be on the order of 3-4 atoms of silicon, including contributions from surface imperfections.[11] Surfaces have become a significant fraction of the device size and can appreciably affect the electronic properties of the device.[12, 13] Therefore, there is a significant impact on device performance from surface variability, which increases current leakage and battery power loss, and ultimately reduces yield due to failed devices.[14] To solve this issue, developing atomic-level processing technologies is imperative, especially for the 7 nm technology node and beyond[15].

Generally, plasma etching and thin film deposition and are quite critical processes in the sub-10 nm fabrication. Conventional plasma etching has limitations to achieving the tight critical dimension control required.[5] However, ALE can achieve atomic-scale thickness controllability, smooth interfaces, and excellent depth uniformity.[16] In terms of deposition, chemical vapor deposition (CVD) and physical vapor deposition (PVD) do not provide sufficient control to achieve ultra-thin, continuous and conformal films on high aspect ratio features.[17] ALD has atomic-scale thickness controllability, good step coverage, and high film density at low deposition temperatures.[18] ALD and ALE are considered to be critical atomic-level processing technologies in the semiconductor industry. However, while ALD has become productive enough to become a mainstream technology, the etch counterpart ALE has been more challenging.

ALD was popularly introduced in 1977,[19] and now has been widely applied in the semiconductor industry. ALE was reported for over 25 years,[20] but it is difficult to provide sufficient productivity to make it suitable for the cost-sensitive manufacturing environment, which has limited its application in the semiconductor industry. In the future, if ALE could overcome this challenge, it would be exclusively used in the semiconductor industry, like ALD.[21-23] This work aims to examine the fundamentals, mechanistic understanding, and potential applications of ALD and ALE in nanofabrication processing.

1.2 Collaborative research

Reaching atomic scale processing for enabling the control of matter at the sub-nanometer level is an interdisciplinary problem that requires collaborative efforts with world-class, interdisciplinary experts in academia and industry.

Carrying out this project at The Molecular Foundry at Lawrence Berkeley National Laboratories, gave me the opportunity to lead my research on atomic scale processing in a scientific stimulating environment. The Molecular Foundry provided an excellent experience for identifying the most crucial applications for Atomic Layer processes. Dr. Deirdre Olynick, Dr. Adam Schwartzberg, and Dr. Stefano Cabrini of the Molecular Foundry worked closely with the researchers at Technische Universität Ilmenau to optimize the research strategy and quality to maximize the impact of this work. The approaches developed at The Molecular Foundry were, in turn, transferred to industrial scale reactors available at Oxford Instruments and Seagate Technology. This was critical in order to ensure that the approaches developed at The Molecular Foundry are transferrable to industrial device fabrication. Additionally, sophisticated characterization tools are available at The Molecular Foundry, e.g. angle resolved spectroscopic ellipsometry, scanning electron microscopy, and X-ray photoelectron spectroscopy. Applying these to the study of ALD and ALE processes and structures complemented this research.

Oxford Instruments Plasma Technology (OIPT) provided valuable feedback and discussion on several topics pertaining to this work. Monthly phone conferences ensured expert feedback and input on the work. Oxford Instruments is leader in semiconductor processing research and provided high-level expertise. The Atomic Layer Etching studies were conducted in collaboration with Dr. Andy Goodyear and Dr. Mike Cooke from OIPT.

Seagate Technology provided unique samples that featured sub-nanometer stacks of materials. The Atomic Layer Deposition studies were conducted in collaboration with Dr. Kim Lee from Seagate. Dr. Kim Lee is a leading expert on magnetic memory fabrication with high skill and expertise.

1.3 Layer by layer fabrication

ALD and ALE have emerged as important techniques for depositing or removing atomically thin films for a variety of applications.[24] Manufacturing processing has been one of the main motivations for the recent development of ALD. The International Technology Roadmap for Semiconductors (ITRS) has included layer by layer fabrication techniques for advanced pattern fabrication.[25] In addition, ALD and ALE have met challenging requirements in other areas including the fabrication of capacitors for DRAM.[26]

Miniaturization in the semiconductor industry has led to the requirement for atomic level control of thin film deposition.[27] Miniaturization has produced very high aspect structures that need to be etched. No other thin film technique can approach the conformality and the aspect ratio independency achieved by ALD and ALE.[28] The necessity for continuous and pinhole-free films in semiconductor devices has driven the advancement of ALD.[28] In addition, the tight control of etching variability offered by ALE is necessary for the fabrication of state-of-the-art semiconductor devices.[12, 13]

1.3.1 Atomic layer deposition

To achieve precision film thickness and conformality, ALD uses the alternation of self-limiting half-reactions.[29] A schematic showing the sequential, self-limiting surface reactions during ALD is displayed in Figure 1.1.

ALD is based on self-limiting surface reactions. Between etch reaction, reactive gases are purged out of the chamber. In general, ALD is most appropriate for binary compounds because a binary chemical vapor deposition reaction can easily be separated into two half-reactions. In the case of metal oxide ALD, the process begins with a hydroxyl-terminated surface and the introduction of a gas-phase metal precursor (Figure 1.1(a)). When a precursor molecule encounters the surface, a rapid chemical reaction displaces one of the precursor ligands (nominally organic, but can also be halides) and a proton from the surface, resulting in a strong metal-oxygen bond. Over time, depending on the temperature, concentration, and reactivity, the surface will saturate and chemistry will cease. The deposition chamber is purged of reactive species, and the second reactive precursor is introduced (Figure 1.1(b)). This is commonly water for the thermal ALD of metal oxides, but plasma-excited oxygen radicals are also used in plasma-assisted metal oxide ALD. The second precursor reacts with the surface-bound species, fully displacing existing ligands

with the new chemistry to form the first layer of reacted material (Figure 1.1(c)). The process involves precursors that are highly reactive with surface species, but inert to self-reactivity at the ALD temperature. In this way, as soon as the substrate has reacted completely with the ALD precursor and saturated any available chemistry, the reaction ceases, despite the presence of excess precursor, thus producing monolayer coverage and conformality.[30]

Following the (b) oxidation step, the surface is back in the original state and is ready for another (a) half-reaction. As a result, the repetition of the half-reactions in an abab... sequence will lead to the deposition materials in an atomic layer-by-layer fashion. The repetitive abab... sequence of these half-reactions can be described as binary reaction sequence chemistry.[31-33] The simple model for binary reaction sequence chemistry assumes that the surface has a finite number of reactive chemical groups. The half-reactions will proceed until all the starting reactive functional groups have been converted into the other functional group. At this point, the surface reaction will limit itself because there are no more reactive sites for additional deposition. In ALD, the precursors transport the elements to the surface, but the ligands on the elements desorb during or soon after the half-reaction. In this case, the atomic layer control of growth occurs because the first monolayer is chemically bound much more tightly than successive monolayers.[34]

The most established and best studied ALD process is thermal ALD in which the surface chemistry is driven solely by thermal energy delivered to the substrate. In most cases, thermal ALD processes rely on H_2O (for metal oxides) as reactants in addition to the metal precursors. However, new ALD methodologies have been pursued in order to expand control over the thermal ALD window, composition and morphology. One approach actively investigated is to supply additional reactivity to the process via non-thermal methods. For example, plasma-activated steps are implemented in the so-called plasma-enhanced or plasma-assisted ALD approach.[34] Additionally, the use of plasma in ALD processes can extend significantly the variety of materials that can be deposited by ALD beyond oxides.

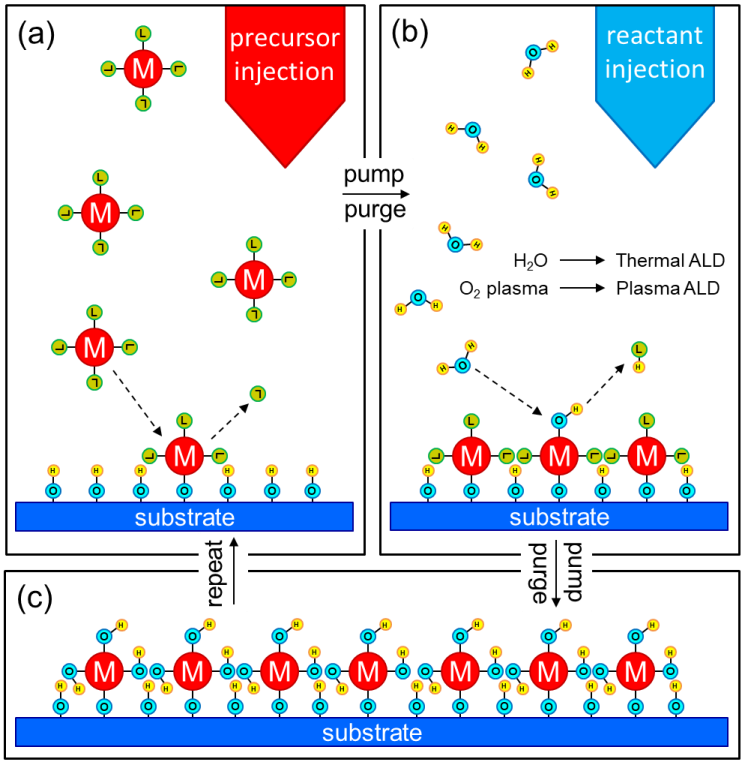

Figure 1.1. ALD precursors are injected into a vacuum chamber and react with hydroxyl terminated surface of the substrate. (a) The chamber is purged of precursor, and a second reactant is introduced that can react with the monolayer of deposited material. (b) The chamber is purged again, leaving a clean, fully terminated monolayer of material. (c) This process is repeated, each step leaving behind a known thickness of material.[29]

The overall ALD thickness is controlled by repeating deposition cycles until the desired thickness is achieved. The growth rate depends largely on the metal precursor, but is generally between 0.3 Å per cycle and 1.5 Å per cycle. It is particularly exciting that different materials can be used in each cycle, allowing one to systematically introduce new atoms at dopant, alloy, or layered-structure concentrations. ALD requires surface functional groups to initiate growth. Consequently, selective ALD can be accomplished by first patterning a substrate with non-reactive species.[35, 36] In addition, ALD provides discrete thickness control, i.e. it has the ability to increase the film thickness layer by layer by repeating ALD cycles. Moreover, ALD film growth is highly uniform and yields excellent conformality because at every available surface site only one precursor/reactant molecule can adsorb regardless of the incoming particle flux. Under optimized ALD conditions, the film growth is therefore independent of whether these surface sites are distributed over a large surface area or in demanding 3D topologies.

For ALD, one clear advantage of *in situ* monitoring (using **in-situ spectroscopic ellipsometry**) can be illustrated by considering the determination of the film thickness and the growth rate per cycle.[37] In turn, this growth rate is employed to predict the number of cycles required to deposit films with the thickness targeted. The importance of in-situ thickness measurement becomes especially clear upon understanding that the growth rate is not necessarily constant during the complete deposition process and often varies with film thickness for ultrathin films. Obviously, the growth behavior of a certain ALD process can be determined much more easily and quickly by acquiring *in situ* data on the film thickness during the deposition process. There is a similar argument for the determination of ALD saturation curves, investigation of the half-cycles and the measurement of optical, structural and even electrical properties of the films.[38, 39] As described in Section 1.5.1 spectroscopic ellipsometry is an optical technique with high sensitivity particularly suited for studies of ALD growth of ultrathin films with submonolayer growth control. In Chapter 3 *in situ* spectroscopic ellipsometry is used to monitor the growth rate of SiO_2 and TiO_2 on serval substrate relevant in the spacer defined double patterning process. In particular, from the increase in film thickness monitored as a function of a number of cycles the growth rate per cycle can be calculated during the ALD process.

1.3.2 Atomic layer etching

Atomic layer etching is a film etching technique that uses sequential self-limiting reactions to remove materials one atomic layer at a time with chemical specificity (Figure 1.2(a)).[16] The simplest ALE implementation consists of two steps: surface modification and removal. Modification forms a thin reactive surface layer with a well-defined thickness that is subsequently more easily removed than the unmodified material. The layer is characterized by a sharp gradient in chemical composition or physical structure of the outermost layer of the material. The removal step takes away the modified layer while keeping the underlying substrate intact, thus "resetting" the surface to a pristine or near-pristine state for the next etching cycle. The removal occurs during the second step, resulting in layer-by-layer material subtraction. The general ALE concept applies to a wide variety of etching schemes which share the same defining ALE criteria: (1) separation into a sequence (cycling) of independent unit process reactions, and (2) at least one step is self-limiting.

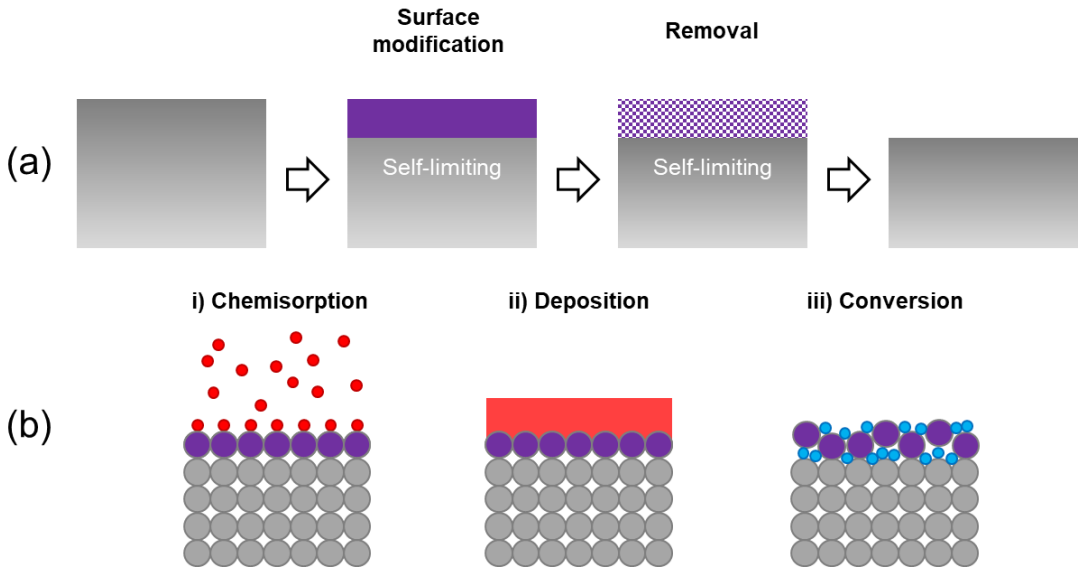

Figure 1.2. (a) Schematic of the generic concept of Atomic Layer Etching. (b) Comparison of different mechanisms to modify the surface in ALE by i) chemisorption, ii) deposition, and iii) conversion.[16]

Separation of reactions means the composite process runs as a repeated series of two or more independent unit steps. In plasma assisted ALE, each step involves distinct chemistry, speciation, and plasma energy composition. ALE processes are developed using a single chamber with sophisticated process control technology to modulate process parameters such as gas composition, gas flow, pressure, and plasma power. The advantage of separation is that it decouples the generation and transport of ions, electrons, and neutrals, thereby increasing access to desirable species fluxes and their relative ratios, i.e., opens the process window. Notably, the primary advantage of separation is that it facilitates self-limiting reactions.

To control the thickness loss (etch depth) per cycle, self-limited surface reactions are required. Both spontaneous chemical etching by the precursor and physical sputtering should be minimal. The ***ALE window*** the process window that allows etching single monolayer per cycle. ALE window is located between the spontaneous chemical etching and the physical sputtering regimes. The key parameter for ALE is ion energy. Figure 1.3(a) shows ALE window versus ion energy. In a plasma environment, ions with an energy distribution are incident on the substrate and control physical sputtering and substrate damage extent. The modification of the surface by the precursor allows the material to be etched with lower activation energy as compared to the underlying material without

modification. The presence of chemical reactants at the substrate surface along with ion bombardment induce a chemical reaction between the surface atoms and the precursor which causes etch products to boil off or sputter from the surface. This process enables directional etching of the material at ion energies above the chemically enhanced etching energy threshold and below the physical sputtering energy threshold. The precursor is chosen so that upon reaction with substrate atoms volatile products can be formed. Conditions must be chosen so that the precursor does not spontaneously etch the substrate, e.g. by lowering the substrate temperature. By carefully tailoring the energy of ion bombardment, it is possible to control the etching depth to about a monolayer. Spontaneous chemical etching of the reactant/substrate system interferes with this approach and the thermal energy required to drive these reactions is made negligible by reducing the temperature of the substrate sufficiently.

Self-limiting reactions refer to those reactions that slow down or stop as a function of time (green curve in Figure 1.3(b)).[40] Self-limiting reactions replace transport-limited reactions of continuous processing, and in this way avoids the associated limitations of continuous etching. For instance, ALE can pattern features independent of aspect ratio. One way to imagine this is as slow reactions (typical of smaller trenches) catching up faster reactions (in bigger trenches) once the etching is complete. As a result, any geometric loading effects that are prevalent in continuous processing are mitigated because the reactions essentially stop.

Experimentally, a variety of self-limiting mechanisms and materials have been reported in literature. Illustrations of different modification mechanisms are shown in Figure 1.2(b), including: chemisorption,[16, 41-51] deposition,[5, 16, 52, 53] and conversion[54, 55] (e.g., oxidation).[52, 53] Removal methods include thermal desorption, particle bombardment, and chemical reaction. A number of these ALE systems use plasma assistance in the modification and/or removal step. All the techniques follow the ALE principles outlined earlier. Ultimately, ALE will be characterized by the following benefits: features with atomically smooth and flat surfaces,[51, 56] reproducibility of stoichiometry,[43, 47, 57, 58] uniformity across the wafer, etching without loading (pattern-density independence), low-damage to remaining material,[41, 58-60] and etch selectivity to other materials. [61]

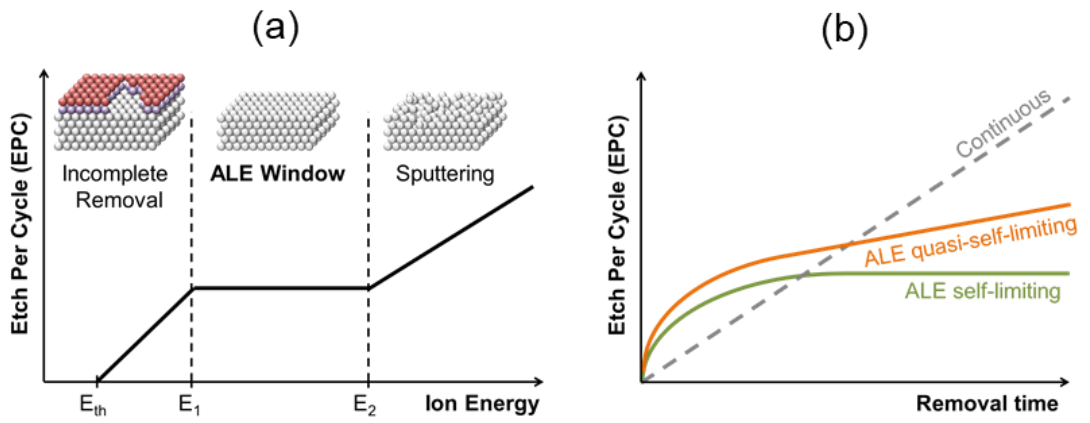

Figure 1.3. (a) Schematic illustrating the concept of an "ALE window" located between the spontaneous chemical etching and the physical sputtering regimes. The presence of chemical reactants on the substrate surface enables directional etching of the material in a window of ion energies above the chemically enhanced etching energy threshold E_{th} and below the physical sputtering energy threshold E_2, respectively. Spontaneous chemical etching of the reactant/substrate system interferes with this approach and is made negligible by reducing the temperature of the substrate sufficiently.[62] (b) "Saturation curves" showing self-limiting removal in (green) ALE (orange) ALE quasi-self-limiting. Self-limitation requires saturation surface coverage. In dashed line, continuous etching is shown for comparable etch time to illustrate lack of self-limiting behavior, which leads to etching strongly dependent on local species fluxes. Even if the continuous process is slowed, by dilution, for example, it is not equivalent to the self-limiting nature of an ALE cycle. [16]

Atomic layer etching is expected to have greater potential than conventional plasma etching to utilize the chemical nature of precursors and thus gain a new level of control over surface reactions. This ability is strongly reduced in continuous plasma processing, and has limited our possibilities of controlling surface reactions by choice of precursor molecular structure. Either exposure of a substrate to precursor gases without plasma or short plasma exposures offer the prospect of retaining a much larger proportion of the precursor molecular structure at the surface, and in this fashion impact etching reactions. The exposure parameters can be varied over a significant range, with steady-state behavior as a limit.

1.4 Material characterization

1.4.1 Spacer Defined Double Patterning (SDDP)

Spacer Defined Double Patterning (SDDP) is a technique used by the semiconductor industry to double the density of an existing prepattern.[63, 64] There are three

major unique features in the double patterning (DP) process we report in Section 2.3.2 for fabrication of bit patterned media: (i) Our prepattern is created using block copolymers (ii) the spacer for the DP is performed using titanium oxide ALD; (iii) SDDP is used to pattern a nanoimprint template instead of active devices.

(i) *PS-b-PMMA Block Copolymers*

Di-block copolymers consist of two immiscible polymeric blocks joined by a covalent bond. They spontaneously phase separate towards a minimum interaction volume driven by a segregation strength, χN, where χ represents the segment-segment Flory-Huggins interaction parameter and N, the degree of polymerization.[65] In block copolymer lithography, a BCP thin film is used in lieu of a resist layer with the self-assembling pattern forming the latent image. Selectively removing one of the two blocks leaves a sacrificial mask that can be used for pattern transfer in a similar way as developed resists are used in conventional lithography.

Spheres, cylinders, and lamellae represent the BCP morphologies most commonly used in lithographic applications.[66] Thin films of lamellae-forming block copolymers where the lamellae orient perpendicular to the substrate are preferred as lithographic materials. Indeed, perpendicular lamellae are more tolerant to thickness variations. Because the domains of perpendicularly oriented lamellae span uniformly from top to bottom with both block materials contacting the bottom of the film, perpendicularly oriented domains are generally better suited for chemical contrast DSA.[67, 68] Additionally, it is also assumed that a uniform profile from top to bottom better resembles a lithographic mask.

Poly(styrene-block-methyl methacrylate) (PS-b-PMMA) is the BCP most likely to be introduced first in a manufacturing environment (Figure 1.4). It has been extensively studied and a large body of creative inventions already exists for domain orientation and directed self-assembly.[69-73] However, the interaction parameter χ is relatively low. Given that segregation strength N for lamellar phase (L_0) needs to be larger than about 10.5 to induce microphase separation and that the pitch scales with N, the achievable dimensions in PS-b-PMMA are limited to about 19-20 nm full pitch,[74] although successful demonstrations of pattern transfer currently stop at 22 nm full pitch indicating that PS-b-PMMA is likely to supply only a partial solution to BPM patterning.

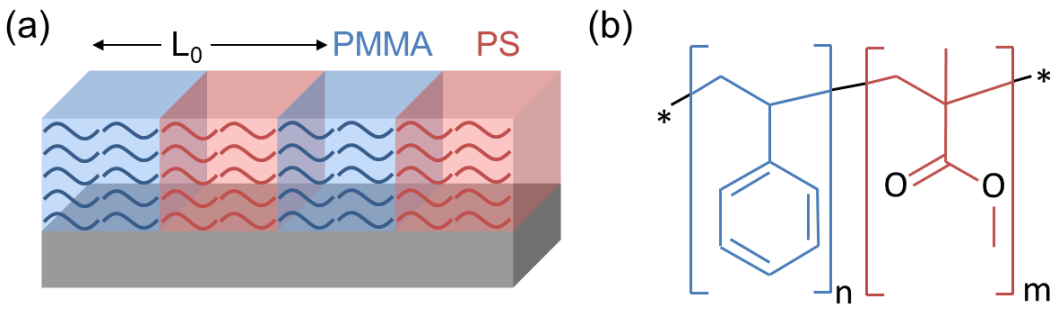

Figure 1.4. (a) Assembly of lamellar Poly(styrene-block-methyl methacrylate) (PS-b-PMMA) (L_0 = BCP pitch). (b) Chemical structure of PS-b-PMMA.[69]

To further subdivide the pitch obtained by PS-b-PMMA block copolymers, an extension of the double patterning (DP) can be readily applied to block copolymer lithography. DP is a manufacturing technique developed to double the feature density. In principle, this provides a path to reach 11 nm full pitch with currently available PS-b-PMMA BCPs. Details of DP patterning will be covered later in this manuscript; here, we only note that the critical dimension deserves special attention when considering BCPs for DP.[75]

(ii) Titanium oxide ALD

ALD is employed to achieve uniform conformal coating of the spacer material on mandrel surfaces. The process should not damage the mandrel, and the spacer material should be dry etchable in an anisotropic manner. The spacer material we use is TiO_2 deposited using thermal ALD at 200 ˚C without plasma assistance. The process used alternating steps of Tetrakis(dimethylamido)titanium (TDMAT) dosing and water vapor oxidation.

(iii) Quartz template fabrication

High volume manufacturing of bit patterned media via nanoimprint lithography requires robust master or sub-master templates usable thousands of times without degradation while withstanding occasional cleaning to remove built-up organic residues or contaminants. The Titanium Oxide features resulting from DP are then applied as the scaffold for pattern transfer into quartz to make a UV nanoimprint mold and further into magnetic storage media.

1.4.2 Silicon oxide

Silicon dioxide (SiO_2) is the most abundant mineral in the Earth's crust. SiO_2 is also an important semiconductor material. SiO_2 has many uses, such as for a gate oxide, interlayer dielectric or spacer, in semiconductor devices. SiO_2 etching is needed for multiple steps during semiconductor manufacturing.[76] There is a wide variety of applications in SiO_2 etching, including the etching of holes such as contact holes and via holes, hard mask etching for gates, and damascene etching. Also, the number of process steps in device manufacturing is the largest among the etching technologies. The progressive miniaturization of semiconductor devices to sub-10 nm dimensions has imposed more demanding requirements on etching. As device structures become increasingly smaller and more complex, high precision etching is necessary at the sub-1 nm level using ALE methods.[11, 77]

SiO_2 etching has a complicated etching mechanism and requires a different type of plasma source. In Chapter 4 I will review the conventional etching mechanism of SiO_2 and then introduce the atomic layer etching for pattern SiO_2 at the atomic scale.

The stack studied primarily for ALE was thermal SiO_2 formed on a silicon substrate by oxidation techniques with 100 nm thickness. Using SiO_2-Si stack allowed for precise thickness measurements via ellipsometer as well as investigating the transition from SiO_2 to Si etching and the potential to achieve SiO_2 over Si etching selectivity.

1.5 Characterization Techniques

Materials and processes were characterized by a variety of techniques including, but not limited to, ellipsometry, atomic force microscopy (AFM), scanning electron microscopy (SEM), and X-ray photoelectron spectroscopy (XPS). Plasma conditions were characterized using an Ion Energy Analyzer and Optical Emission Spectroscopy.

1.5.1 Spectroscopic ellipsometry (SE)

In atomic layer processing, the precise and accurate measurement of the deposited and etched depths is critical for the calculation of the process characterization. Ellipsometry is an optical technique for surface and thin films analysis. It is based on the measurement of the change in polarization state of a light beam caused by the reflection on the material

surface or the transmission through the material. From the change in state of polarization one can deduce film thickness and optical properties of the material.

Ellipsometry measures the change in the state of polarization of a light beam caused by the reflection on the sample surface.[78] The measured parameters are the so-called ellipsometric angles Ψ and Δ. They are related to the ratio of the complex Fresnel reflection coefficients r_s and r_p. Thereby, r_s is the reflection coefficient for light polarized perpendicular to the plane of incidence and r_p is the reflection coefficient for light polarized parallel to the plane of incidence. This is expressed by the fundamental equation of ellipsometry:

$$\rho = \frac{r_p}{r_s} = \tan\Psi \, e^{i\Delta} \qquad \text{(Eq. 1.1)}$$

Film thicknesses evolution in Chapter 3, 5 and 6 were studied using ellipsometry. Based on phase modulation technology, the ellipsometer provides a powerful optical design to continuously cover the spectral range from 190 to 2100 nm. Measurements were performed in Ψ-Δ space, corresponding to changes in phase and relative amplitude of the polarized light source (Xenon arc lamp of 75 Watt with a spectral range from the near IR to the UV). Optical multilayer modeling was used for interpretation of recorded data and to establish real-time thickness changes of various films. Ellipsometry is a highly accurate and precise metrology technique because it measures the change in the state of polarization (expressed by the ratio of reflection coefficient magnitudes and difference in phase change) rather than simply intensity. In addition, ellipsometry is an area-averaging technique, i.e. the measurement is averaged over the area of the laser spot on the sample. Therefore, surface roughness on a smaller scale than the size of the laser spot can impact the measurement and is taken into account.

The collected data of an ellipsometry measurement are the intensities of the change of polarization of the reflected signal in a predefined spectral range. This data are mathematically treated to extract Ψ and Δ. These values are not material parameters or thicknesses thus ellipsometry is an indirect technique of measurement. To extract parameters of interest like optical constants and thickness from the measurement a model has to be set up that allows theoretical calculation of Ψ and Δ. The optical constants can be expressed in the refractive index n and extinction coefficient k, but they are often

represented in terms of the real (ε_1) and imaginary (ε_2) parts of the complex dielectric function ε. The latter are related through the definitions $\varepsilon_1 = n^2 - k^2$ and $\varepsilon_2 = 2nk$.

The raw data obtained from the measurements contain the change in polarization caused by the interaction of the light with the (multi-layered) sample and are often expressed in the parameters Ψ_{exp} and Δ_{exp} or the pseudo-dielectric function ε_{exp}, which are related via

$$\varepsilon = \varepsilon_1 + i\varepsilon_2 = \sin^2(\phi)\left[1 + \left(\frac{1-\rho}{1+\rho}\right)\tan^2(\phi)\right] \qquad \text{(Eq. 1.2)}$$

where the angle of incidence is given by ϕ and the quantity ρ is defined by (Eq. 1.1). Ellipsometry software is used to calculate the optical response of all the layers combined into the ellipsometric parameters Ψ_{mod} and Δ_{mod} of the model. The goodness-of-fit, i.e. the extent to which the model describes the experimental data, is expressed by the difference between the simulated and experimental data. The parameters of interest are determined by a comparison of theoretical and experimental data, the true optical constant values of the different parts composing the sample structure.[79, 80]

With spectroscopic ellipsometry (SE), a new Ψ_{exp} and Δ_{exp} are measured at each wavelength within a measured spectrum. Dielectric materials, i. e. (i) TiO_2 (Chapter 3) and (ii) SiO_2 (Chapter 5), are transparent over a wide spectral range from IR to deep UV. The measurement of these materials can be done over a very broad part of the spectral range because they are transparent from IR to UV and even deep UV. Ellipsometric measurements from IR to UV provide a wealth of information. Silicon dioxide, for example, is transparent for wavelengths > 250nm. When the film is transparent, $n = f(\lambda)$ and $k = 0$, The wavelength is independent of thickness. Under this transparency condition, n and film thickness can be fit for multiple layers in a stack even if the layers are different compositionally and structurally.

Optical dispersion means dependence of optical properties on wavelength or photon energy. Sometimes this dependence can follow an explicit analytical formula, called dispersion formula. These dispersion formulae mostly are physically related to optical transitions in materials, however, they also can be purely empirical without any physical meaning.

(i) Titanium oxide -TiO_2 (Chapter 3)

TiO_2 is an indirect bandgap material with an optical gap around 3.0–3.5 eV depending on its crystalline phase.[81, 82] The bandgap of amorphous TiO_2 is somewhat lower than the 3.4 eV reported for anatase TiO_2, but higher than the typical bandgap of 3.0 eV for rutile TiO_2.[83, 84] A Tauc–Lorentz double oscillator model has been used to describe the TiO_2 dielectric function.[85] The Tauc–Lorentz oscillator model is given by:[86, 87]

$$\varepsilon_2(E) = \sum_{j=1}^{n} \frac{A_j E_{0j} \Gamma_j (E-E_{gj})^2}{(E^2-E_{0j}^2)^2+\Gamma_j^2 E^2} \cdot \frac{1}{E} \qquad \text{(Eq. 1.3)}$$

In (Eq. 1.3), E_{gj} represents the bandgap, E_{0j} is the peak transition energy, Γ_j is the broadening parameter and A_j represents the optical transition matrix elements.

(ii) Silicon oxide - SiO_2 (Chapter 5 and 6)

Silicon oxide has an optical bandgap of ~8. 8 eV and is, as a consequence, non-absorbing ($k = 0$) over the total photon energy measurement range of ellipsometers commonly applied. Therefore, a standard Cauchy relationship can be used to describe the dispersion of the refractive index n:[81]

$$n = A_n + \frac{B_n}{\lambda^2} + \frac{C_n}{\lambda^4} \qquad \text{(Eq. 1.4)}$$

in which A_n, B_n and C_n are the Cauchy fit parameters that are often represented for wavelength λ in micrometer units.

The film thickness of materials is determined by interference between light reflecting from the surface and light traveling through the film. Depending on the relative phase of the rejoining light to the surface reflection, interference can be defined as constructive or destructive. The interference involves both amplitude and phase information. The phase information from Δ is very sensitive to films down to sub-monolayer thickness. There are large variations in Δ, while the reflectance for each film is nearly the same.[88] Ellipsometry is typically used for films whose thickness ranges from sub-nanometers to a few microns. Thickness measurements also require that a portion of the

light travel through the entire film and return to the surface. If the material absorbs light, thickness measurements by optical instruments will be limited to thin, semi-opaque layers. This limitation can be circumvented by targeting measurements to a spectral region with lower absorption. For example, an organic film may strongly absorb UV and IR light, but remain transparent at mid-visible wavelengths. For metals, which strongly absorb at all wavelengths, the maximum layer for thickness determination is typically about 100 nm.[89]

1.5.2 Scanning electron microscopy (SEM)

The scanning electron microscope (SEM) produces images by scanning the sample with a high-energy beam of electrons. As the electrons interact with the sample, they produce secondary electrons, backscattered electrons, and characteristic X-rays. These signals are collected by one or more detectors to form images which are then displayed on the computer screen. When the electron beam hits the surface of the sample, it penetrates the sample to a depth of a few microns, depending on the accelerating voltage and the density of the sample. Many signals, like secondary electrons and X-rays, are produced as a result of this interaction inside the sample. The maximum resolution obtained in an SEM depends on multiple factors, like the electron spot size and interaction volume of the electron beam with the sample. While it cannot provide atomic resolution, some SEMs can achieve resolution below 10 nm. Typically, modern full-sized SEMs provide a resolution between 10 and 20 nm.

In this work surface morphology, pattern distortion, and process directionality were characterized using the Zeiss Ultra 60 Scanning Electron Microscope which uses the good imaging capabilities of the GEMINI® field emission column (FESEM). The In-column EsB (Energy selective Backscatter) detector is less sensitive for edge contrast and charging effects which enables precise feature imaging and reliable metrology. The Zeiss Ultra 60-SEM delivers superb materials contrast and crystallographic imaging. As a trade-off between resolution and beam damage, samples were imaged using a Zeiss Ultra 55 field emission scanning electron microscope (FESEM) at an acceleration voltage of 7 keV, beam current of 190 pA, with a 30 µm aperture (on axis) and at 3.7 mm of working distance (WD).

1.5.3 X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) analysis provides information on the chemical composition of the film surface. The analysis was performed using K-Alpha Plus

XPS/UPS. The analysis system consists of a monochromatic Al X-ray source with variable spot size ranging from 30 microns to 400 microns, a combined low energy electron/ion flood source for charge neutralization, a dual monoatomic and gas cluster ion source for depth profiling and sample cleaning, and an ultraviolet light source (He1 and He2) for probing valence states and work function of material surfaces. Narrow scan spectra of the Si2p, C1s, O1s, and F1s were obtained. Spectra were fitted using a least square fit after background subtraction. All fittings were required to show consistency across all individual spectra, i.e. the chemical information extracted from Si 2p, C 1s, O 1s, and F 1s was internally consistent.

1.5.4 Ion Energy Analyzer

In a collisionless dc discharge, the IED hitting a surface is expected to be monoenergetic with energy $e\bar{V}_s$, where $\bar{V}_s$ is the dc sheath voltage drop. In rf discharges, however, there can be large ion energy spreads due to ion modulation in the time varying sheath potential. In collisionless rf sheaths, the crucial parameters for determining the IED are the ion transit time across the sheath, τ_i, and the sheath rf period, τ_{rf}. The ion transit time is calculated from $\tau_i=3\bar{s}\sqrt{m_i/(2e\bar{V}_s)}$, where $\bar{s}$ is the time averaged sheath width and m_i is the ion mass. When $(\tau_i/\tau_{rf}\ll1)$ the ions cross the sheath in a small fraction of the rf cycle and the final ion energies depend strongly on the phase of the rf cycle in which they enter the sheath. This results in a broad bimodal distribution with the width of the IED, ΔE, almost equal to the maximum sheath drop. Conversely, when $(\tau_i/\tau_{rf}\gg1)$ the ions take many rf cycles to cross the sheath and are not able to respond to the instantaneous sheath voltage. The phase at which the ions enter the sheath becomes unimportant and results in a narrowing of the IED. In this high frequency regime $(\tau_i/\tau_{rf}\gg1)$, the ΔE of the IED has been calculated by Benoit-Cattin and Bernard.[90] This is quite a simple model but will suffice to aid understanding of the results presented in the following section. We assumed:

(i) a constant sheath width,
(ii) a uniform sheath electric field,
(iii) a sinusoidal sheath voltage, $V_s(t)=\bar{V}_s+\tilde{V}_s\sin\omega t$
(iv) zero ion velocity at the plasma-sheath boundary.

The resulting expressions for ΔE and IED are:

$$\Delta E = \frac{4e\tilde{V}_s}{\pi}\left(\frac{\tau_{rf}}{\tau_i}\right) \qquad \text{(Eq. 1.5)}$$

and

$$f(E) = \frac{2n_t}{\omega \Delta E}\left[1 - \frac{4}{\Delta E^2}\left(E - e\tilde{V}_s\right)^2\right]^{-1/2} \qquad \text{(Eq. 1.6)}$$

where n_t is the number of ions entering the sheath per unit time and $\tilde{V}_s$ is the amplitude of the rf component of the sheath voltage. The result of the calculation is a bimodal distribution centered at $e\tilde{V}_s$ which has a peak separation ΔE proportional to τ_{rf}/τ_i.

Time resolved plasma properties were characterized using a Semion - Retarding Field Energy Analyser (RFEA) from Impedans Ltd. In a retarding field analyzer a series of grids are used to select particles having a given charge sign, and to analyze the energy distribution of these particles. Depending on the grid biasing, the analyzer can be configured to measure the energy distribution of either ions or electrons. The most usual application of the RFEA is to measure ions from the plasma, which are accelerated toward the analyzer entrance by the sheath field. The Semion from Impedans Ltd measures the ion energy and produces the ion energy distribution function (IED), ion flux, negative ions, temperature and DC bias at the substrate position inside a plasma reactor.

The RFEA was performing a series of five consecutive scans automatically. All the data recorded were then averaged and plotted to increase the signal to noise ratio. The IED curves sowed in section 5.3.1 and 6.3.2 are collected using the aforementioned technique.

1.5.5 Optical Emission Spectroscopy

Optical Emission Spectroscopy (OES) is the most widely used diagnostic technique in plasma etching. The vast majority of optical emission in etching plasmas is a result of electron-impact excitation. Plasma is an ionized gas under pressure and subjected to intense heating or electromagnetic fields to the point that electrons and positive ions are unbound. Plasma is one of the four fundamental states of matter, but it does not exist on Earth naturally and must be generated by applying heat and pressure. What makes plasma unique from other states of matter is its behavior. The speed of atoms in a plasma is higher than in a gas. This movement of charged particles creates an electric current within a magnetic field, and while the overall charge of a plasma is usually neutral, it is also highly

conductive. Because of the complexity of the excitation mechanism, OES is usually a qualitative technique.

In order to characterize the plasma parameter during atomic layer etching of SiO_2, the plasma emission spectra were collected in real time from the plasma chamber using a USB2000 spectrometer from Ocean Optics.

1.6 Thesis Outline

The main goal of this work is to establish and characterize processes to enable control of matter at the atomic level. Fundamental mechanisms behind ALD and ALE are identified.

Chapter 2 introduces the reader to the concept of miniaturization in the semiconductor and hard disk drive industries. The critical dimension scaling toward the sub-10 nm node requires the fabrication of several-nanometer sized features with atomic scale fidelity. *Inter alia*, the multiple patterning technique is introduced as one of the most powerful methods for scaling dimensions beyond the lithography resolution limit.

With specific attention to the hard disk drive industry, Chapter 3 shows how to increase data storage densities beyond 5 Tb/in^2. A predominate route towards single-bit combines lithographically directed self-assembled block copolymers and Spacer Defined Double Patterning via atomic layer deposition (ALD). The fabrication of structures at 7.5 nm half-pitch and below using the spacer defined double patterning is demonstrated, thanks to a deep understand of the material creation and characterization. With the goal of achieving a dense pattern with good mechanical stability, ALD chemistry and process conditions are essential to controlling the process and can only be achieved through an in-depth understanding of materials and their interactions.

The second part of this work presents ALE of SiO_2 in a conventional inductively coupled plasma etching tool supplied by Oxford Instruments. This work provides defining criteria for ALE of SiO_2, along with the establishment of the impact of plasma parameters on the etch performance. First, conventional plasma etching methods for patterning SiO_2 features are discussed. Chapter 4 shows the mechanism beyond conventional

Fluorocarbon-based etching and explains the limitation of using continuous plasma processing as well as introduces the concept of fluorocarbon-based ALE.

A deep understanding of the plasma-surface interaction and the binding energy of the surface atoms is necessary for developing and understanding a reproducible etching process. As shown in Chapter 5, using sequential reaction steps that are self-limiting, it is possible to remove few-angstroms-thick layers of SiO_2. Experimental studies have paved the way to establish cyclic CHF_3/Ar plasma capable of ALE of SiO_2. Self-limited removal of Ångstrom-thick layers of SiO_2 based on periodic, precise precursor injection in conjunction with synchronized low energy Ar^+ ion bombardment is demonstrated. Ellipsometry is used to measure thicknesses and etch rate. Chemically enhanced etch rates are observed as long as F is present at the surface. Maximum ion energies are below the physical sputtering energy threshold, leading to a self-limited removal. Chapter 6 extends this cyclic ALE approach to SiO_2 features patterning. The three process parameters FC film thickness deposited per cycle, maximum ion energy, and etch step length are explored. Ultimately, the ability to achieve aspect ratio independent etching is demonstrated, establishing the potential of the developed cyclic atomic layer etching process for atomic scale device pattern transfer.

Finally, the main conclusions of this work are summarized. Additionally, future work and possible directions of the semiconductor industry are outlined and discussed.

Chapter 2

Miniaturization in the Semiconductor industry and Bit Pattern Media

Overview

This chapter introduces the concept of miniaturization in manufacturing, starting with the transition from millimeter to the atomic scale. In order to understand the general evolution of the feature size scaling and the transition to the atomic regime, the change in critical dimension and hard disk drive bit size are shown over time. Dimension scaling trends require the fabrication of sub-10 nanometer features with atomic scale fidelity. To understand the importance of pattern fabrication in manufacturing, a comparison of nanofabrication methods and their state-of-the-art critical dimensions are shown. At nodes below 10 nanometers multiple patterning is introduced for line pitch scaling. This innovative approach relies on an increasing number of deposition and etch steps to achieve dimensions beyond the lithography resolution limit.

2.1 From the millimeter scale to the atomic scale

The micron, nano, and atomic length scales range from 10^{-3}-10^{-6}m, 10^{-6}-10^{-9}m, and 10^{-9}-10^{-10}m respectively. However, in terms of nanotechnology, the definitions are modified. Figure 2.1 helps visualize the dimensional separation at small length scales and compares some commonly known objects down to the atom. The micron-scale ranges between 0.5 μm and 100 μm, while for the nanoscale is less clear where to set the boundaries.[91]

Nanoscience is widely defined as the study of phenomena and manipulation of the matter at the atomic, molecular and macromolecular scales. At dimension lower than 500 nm, the material properties significantly change from those at larger scale and novel application rises from size-dependent phenomena. For example, at the nanoscale, surface becomes more import that volume.[92] However, entering in the sub-10 nm dimension sizes requires new definitions at the lower limit of the nanoscale.[93-96]

The term sub-10 nm scale describes the length scale between 1 nm and 10 nm. Below the sub-10 nm scale,[97] the atomic scale is used for describing lengths of the sizes of atoms, which is between 1 Å and 1 nm.[98] Sub-10 nm scale and atomic scale objects have been successfully fabricated and integrated with functional devices at laboratory level using several approaches. Yet the transfer of these technologies from laboratories to manufacturing is not straightforward. In fact, manufacturability implies that reproduction of these nano-objects is possible with limited variations of their structural or functional properties. The intrinsic level of variability of the current fabrication processes calls into questions the possibility to further extend them into the atomic range. Consequently fabricating the small, complex, functional components that future applications may require will necessitate the introduction of novel methodologies or the integration of new technologies in current fabrication processes.[99]

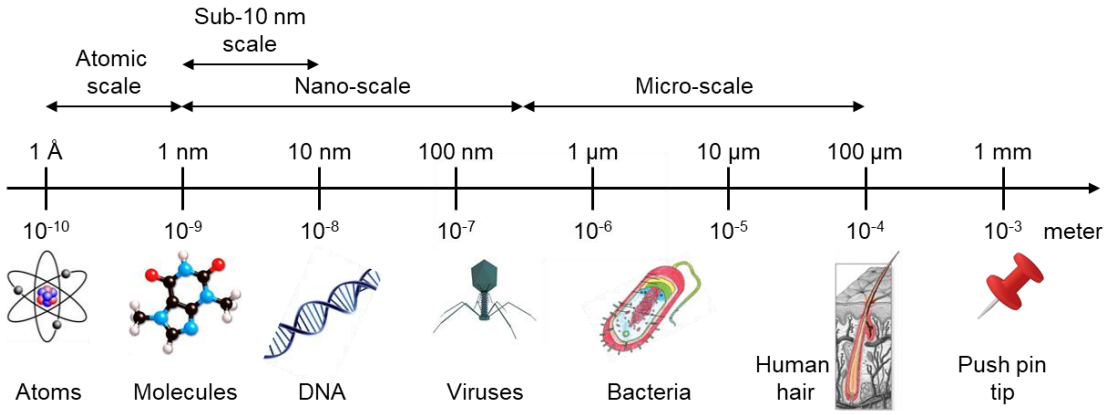

Figure 2.1. Dimension at the logarithmic scale compared to some known objects. Atoms: 1 Å to 5 Å; molecules: 5 nm; DNA: 40 nm to 80 nm; Bacteriophage virus: 200 nm tall; bacteria: 4-7 µm; diameter human hair: 15-200 µm; pushpin tip: 0.8-1.2 mm in diameter.[91, 92, 98]

2.1 Nanofabrication scaling trend

Nanotechnology is characterized by its comminutes trend of scaling down the fundamental dementias. Structures and featured become smaller, while total area typically become larger. This trend keeps new technology available, reducing manufacturing pricing. The scaling down of critical dimension, however, cannot continue forever but will end when it reaches the single atom. Therefore the final frontier of scaling will be in the atomic scale, where every single atom counts.[100]

Scaling down of the CD for manufacturing has always been accompanied by the need for innovation and improvements in processes and methods. Every attempt to decrease the dimension of a structure requires process changes, new fabrication methods, and higher process control. In order to predict and extrapolate possible future development, it is necessary to look at past and recent trends in different technologies.

The trend of scaling down over time can be visualized to clarify the need for further progress in the near future. The downscaling for planar technology only take into consideration the two lateral dimension, while the z-dimension is easily modulated by deposition whereas the lateral dimension requires a lithographic step. Here, the scaling in the Semiconductor industry and Hard Disk Drive industry are introduced.

2.1.1 Semiconductor industry scaling

The central processing unit (CPU) utilized in semiconductor industries has circuitry with nanometer feature dimensions. Logic structures are made of transistors as well as connecting wire metallization with dimensions in the micro- and nanoscale range. Crucial for the semiconductor industry is the engineering of electrical properties, which are determined by distances. For example,[101] the pitch and the feature width become dominant in CPU fabrication. Therefore, for a reduction of the total area size, all components have to be reduced in size. However, critical dimensions like gate length and gate oxide thickness determine the fabrication limits.

Early in the 2000s, semiconductor scaling encountered fundamental physical limits that now make it impractical to continue along the historical paths to ever-increasing performance.[102] Figure 2.2 graphs the history of Intel chip introductions by clock speed and number of transistors.[103] Expected improvements in both performance and power achieved with technology scaling have slowed from their historical rates, whereas implicit expectations were that chip speed and performance would continue to increase dramatically.[104] There are deep technical reasons for why the scaling worked so well for so long and why it is no longer delivering dramatic performance improvements. In the past, computer architects increased performance with clever architectural techniques such as instruction-level parallelism. As the number of transistors per unit area on a chip continued to increase (as predicted by Moore's Law),[105] microprocessor designers used these transistors to increase the potential to exploit parallelism by increasing the number of instructions executed in parallel.[106] Transistors were also used to achieve higher frequencies than were supported by the raw transistor speedups, for example, by duplicating logic and by reducing the depth of logic between pipeline latches to allow faster clock cycles. Both of these efforts yielded diminishing returns in the mid-2000s. Figure 2.2 also illustrates how gains in frequency and single-thread performance have stagnated in recent years.

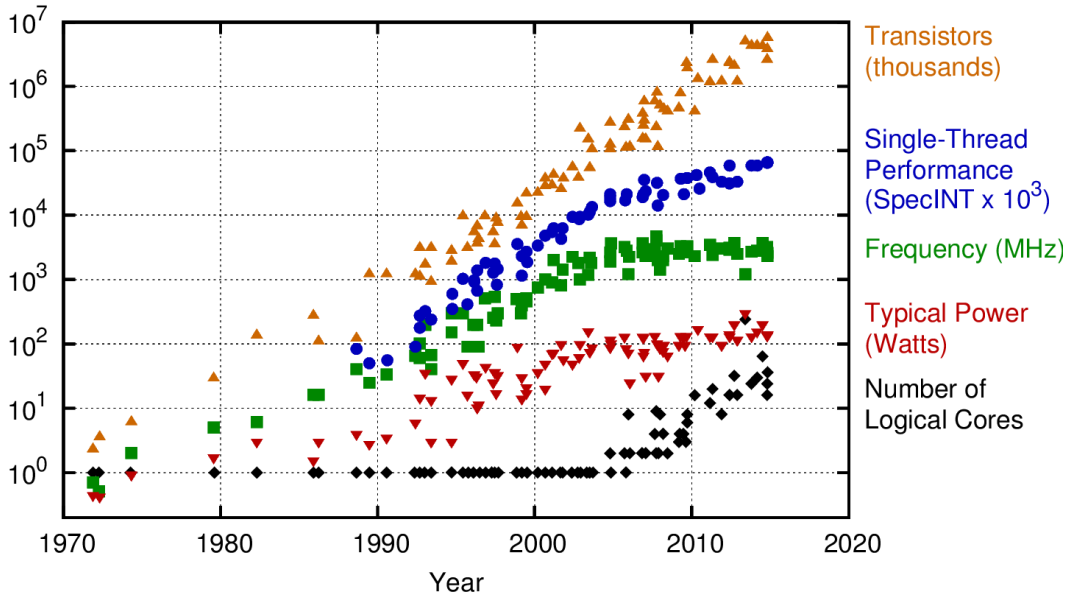

Figure 2.2. Intel CPU Introductions (graph updated 2018). Microprocessors trend data over the past 40 years CPU scaling showing transistor density, power consumption, and efficiency. Source: [103].

Continuing the progress of semiconductor scaling—whether used for multiple cores or not—is now dependent on innovation in structures and materials to overcome the reduced performance scaling. Continued scaling also depends on continued innovation in lithography. As reported in Chapter 4, current state-of-the-art manufacturing uses a 193-nanometer wavelength to print structures that are only tens of nanometers in size. This apparent violation of optical laws has been supported by innovations in multiple patterning and compensated for by increasingly complex computational optics.

Future lithography scaling is dependent on continued innovation. In fact, scaling of semiconductor technology hit several coincident roadblocks that led to this slowdown, including architectural design constraints, power limitations, and chip lithography challenges. The combination of these challenges can be viewed as a perfect storm of difficulty for microprocessor performance scaling (Figure 2.2). Due to increased complexity in transistor design, and in order to ensure advancing in technology node, feature diminution must decrease. A forecast by the international roadmap of semiconductor is expected to reach 6 nm in 2024. Overall all feature dimensions will reach the sub-10 nm scale within the next ten years.

2.1.2 Hard Disk Drive scaling – Bit Patterned Media (BPM)

The advent of the digital electronic device created the need for digital recording.[107] The key concept of digital magnetic data storage is the ability of a media to be in only two well defined magnetic states, corresponding to a binary digit.[108] Magnetic material with uniaxial anisotropy has very well defined states because their magnetization can be flipped by the application of a magnetic field.[109-111]

The demand for storage increases due to the amount of information that has been generated. In fact, data volume is now doubling every two years, creating a great opportunity for the hard drive industry to increase the amount of data that can be stored in a hard disk drive (HDD).[112] The growth in information is driven by three main areas[113]:

a) Videos: e.g. YouTube
b) Big data analysis: e.g. big corporations, banks
c) Mobile applications: e.g. personal music, video, pictures

The best state for meeting this demand is not to build more drives, because it would imply 15-200 times expansion of HDD factory capacity and would be too expensive. Moreover, the big software companies (Google, Facebook, Amazon, Apple, Microsoft, etc.) would need to build more servers and data centers, again at too high a cost.[114, 115] For this reason, the right way to accommodate this new volume of data is to increase the areal density of the media, and so drastically increase the data density.[116]

Figure 2.3 shows the Advanced Storage Technology Consortium (ASTC) road map for magnetic recalling technology.[117] As shown, perpendicular magnetic recording (PMR) is going to a plateau at 1.5 Tb/in^2. Heat-assisted magnetic recording (HAMR) will naturally follow PMR. Indeed these two techniques are similar in terms of equipment and materials and so HAMR has little added cost in terms of investment in infrastructure and equipment. But again, heat-assisted technique uses a granular media and so it is also subjected to the paramagnetic limit.[118] The only way to have areal density beyond 1 Td/in^2 is to transition toward Bit pattern media (BPM).[119, 120]

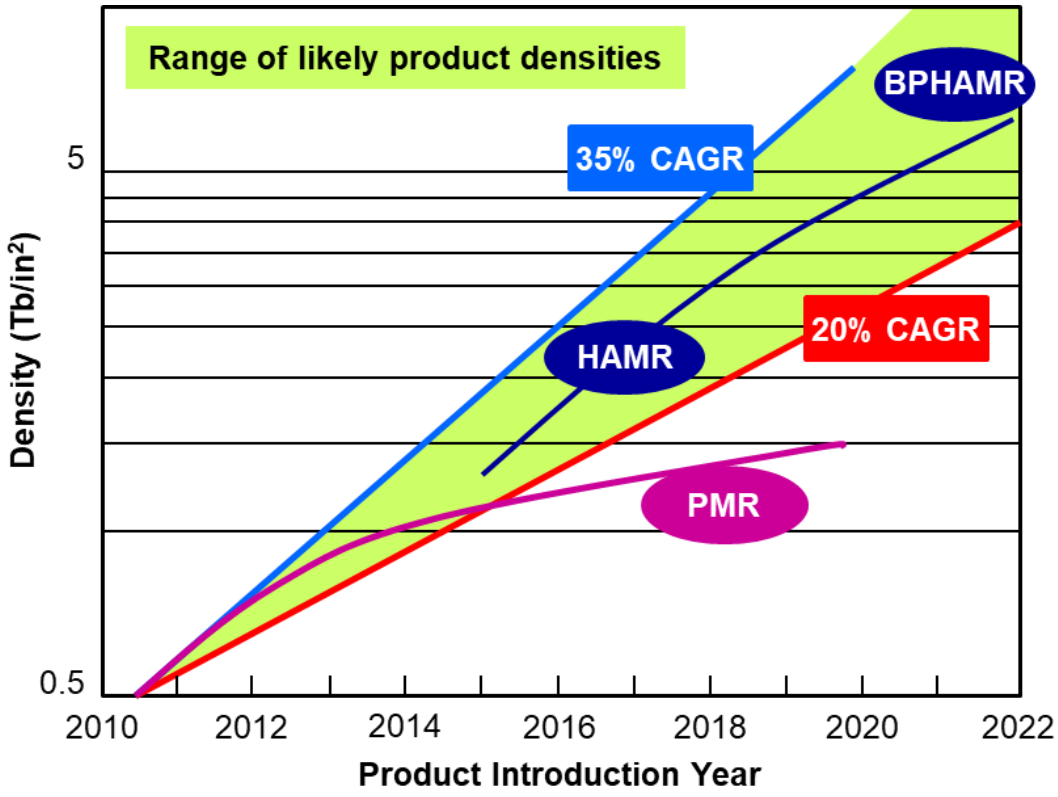

Figure 2.3. Road map for magnetic memories. Since the demand for recording density of Hard Disk (HD) is increasing, the magnetic data storage media will evolve from the recording layer structure of perpendicular magnetic recording (PMR) into new technologies. BPM: Bit-Patterned Media; HAMR: Heat-assisted magnetic recording. The global non-volatile memory market is anticipated to expand at a Compound Annual Growth Rate (CAGR) between 20 % and 35 % during 2010-2022.[117]

In a granular pattern media, each bit consists of several crystalline grains, and in the technology used by Seagate Technologies each bit contains about 14 grains.[121] For the BPM instead, the starting point is a continuous media, then using a combination of hard masks and etching techniques it is possible to create a regular array of bits.[122-124] Each single island-bit ideally contains one single grain, increasing the volume of a single grain while decreasing the size of each individual bit.[120]

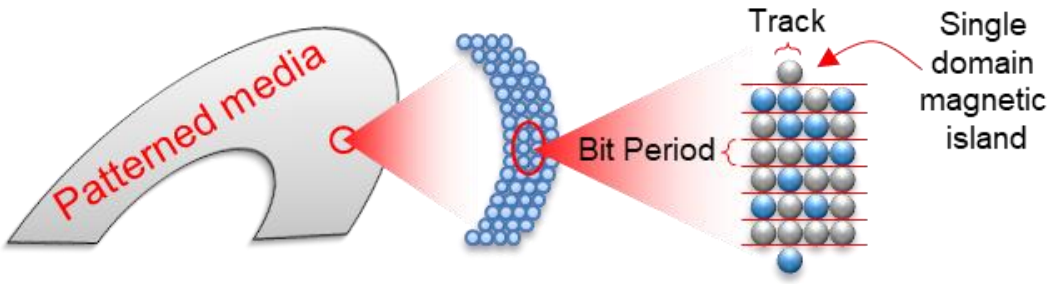

Figure 2.4 Patterned media replace the many random grains of conventional, continuous thin-film media with one large magnetic island that stores a single bit. The bits can then be scaled to a smaller size, allowing higher density while remaining thermally stable.[125]

The concept of BPM is to pattern a magnetic film into individual islands, where each magnetic island stores one bit.[126, 127] Figure 2.4 shows a schematic of bits stored in BPM. As the bit boundaries are defined physically by the boundary of each island, the original film can be deposited so that there is strong exchange coupling between the individual grains within an island.[66, 125] This coupling allows the size of a bit to be decreased, maintaining thermal stability and producing an adequate signal-to-noise ratio.[103] If introduced using conventional write-head technology, BPM is estimated to enable areal densities up to 5 Tb/in^2.[128] However mass producing arrays of nano-sized magnetic islands is not an easy task, and the requirements placed on their properties are stringent. The topographical requirements are that the placement and size of each bit must be precise. Accurate placement is required to achieve write synchronization between the read/write-head and the underlying bits.[126, 129] Bit size must not be so great that adjacent bits touch and magnetically couple, and not so small that the bit becomes superparamagnetic.[130]

Table 2.1 summarize the challenges for the bit pattern media.[131] The areal density is related to both the bit size and the pitch size of the pattern. The areal density of 2 Tb/in^2 and below can be reached using bit size of at least 9 nm. In this way it is possible to overcome the limitations of granular media that set the maximum areal density at 1.5 Tb/in^2. But the patterning required for this high areal density creates tremendous challenges for lithography and, of course, for pattern transfer in magnetic media. Moreover, it is also important to control the position and size of magnetic boxes with a maximum mismatch of 5% from the nominal values.[127, 132] The final challenge is maintaining the path: perpendicular magnet media is a cheap technique and so low manufacturing cost it is also an important issue.

Table 2.1. Bit patterned Media challenges: required lithography dimensions for various areal density.[131]

Areal density [Tb/in^2]	Bit size [nm]	Pitch size [nm]
1	13	25
1.5	10	20
2	9	18
5	6	11
10	4	8

Fabrication of BPM diverges significantly from nanofabrication processes practiced by the semiconductor industry for multiple reasons: 1) BPM features sizes (generally < 20 nm full pitch in the down-track direction) are beyond the capability of conventional lithographic methods; 2) BPM requires single-shot full-disk lithography to avoid stitching errors; 3) BPM patterns are circular in nature and highly periodic; 4) target costs are much lower and total area to be patterned is much larger than for semiconductors; 5) BPM can tolerate a relatively high defect rate (~10^{-3} defective islands). Taking these factors into account has led to the development of a new fabrication process as described in Section 2.2.2.

2.2 Sub-10 nm fabrication

Nanofabrication is characterized by the continuous reduction of critical feature dimensions, which affects the entire manufacturing process, including lithography, imaging and pattern transfer. With feature sizes approaching or below the sub-10 nm regime, the number of available technologies capable of meeting resolution requirements decrease. The goal of this work is to provide solutions in the fabrication of nanofeatures during the pattern transferring step. Indeed, improvements in plasma etching transfer and in defining sub-10 nm features are essential for future nanofabrication.

2.2.1 Pattern transfer

Pattern transfer can be divided into additive, subtractive (etching) and a combination between both (multiple patterning). Purely additive methods are unable to meet the critical dimension needed. Wet etching is a subtractive technique that will not be mentioned here as its resolution is limited to the microscale.[1] Therefore, only subtractive

methods (Chapter 4) or combinations in multi-patterning (Section 2.2.2) are usable for pattern transfer at the sub-10 nm scale.

Plasma etching will be largely discussed in Chapter 4 as the preferable method to pattern transfer in the semiconductor device fabrication. Therefore, the two most relevant methods for sub-10 nm nanofabrication are continuous plasma reactive ion etching (RIE) and atomic layer etching (ALE). In ALE, the etching rate approaches one atomic layer per cycle, where the atomic layer thickness is not necessarily one monolayer of the substrate but rather the reacted layer. After etching, the substrate surface remains (atomically) smooth and it is possible to achieve the ideal condition of removal of exactly one monolayer of the substrate per cycle.

2.2.2 Multiple pattering

The simplest form of multiple patterning is double patterning, which increases feature density by a factor of two. In this scheme, spacers are formed on the sidewalls of a pre-defined feature, called a mandrel, through deposition and etch process steps. Next, the mandrel is removed by an additional etch step, leaving only the spacers, which are then used to define the desired final structures. Because there are two spacers for each mandrel, the feature density is doubled. One attribute of the spacer technique is that, in principle, it can double the pattern density indefinitely by repeating the spacer formation and pattern transfer steps. For example, doubling a double patterning scheme results in quadruple patterning. While double patterning with current 193 nm immersion lithography can achieve a half-pitch resolution of ~20 nm, quadruple patterning can achieve a half-pitch resolution of ~10 nm (Figure 2.5). With such small feature dimensions, minimizing variability of the enabling deposition and etch steps is critical. To allow continued scaling, production-worthy processes that deliver atomic-scale control, such as atomic layer deposition, are becoming even more important.

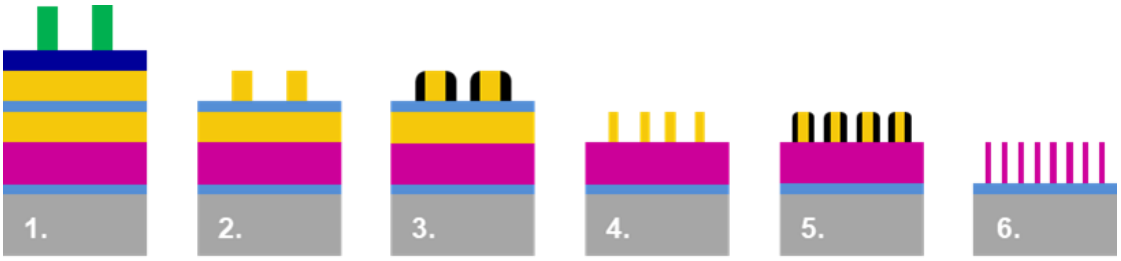

Figure 2.5 Schematic illustration of the standard SAQP approach, in which two hard mandrels are used (associated with the appropriate etch stop and hardmask layer). This integration is complex and involves several sacrificial layers that require multiple dry- and wet-etch steps: **1.** Lithography; **2.** Etch top mandrel; **3.** Deposition and etching spacer 1; **4.** Remove top mandrel, etching bottom mandrel; **5.** Deposition and etching spacer 2; **6.** Remove bottom mandrel, etching final pattern. In this scheme, spacers (in back) are formed on the sidewalls of a pre-defined feature, called a mandrel (in yellow), through deposition and etch process steps. Next, the mandrel is removed by an additional etch step, leaving only the spacers, which are then used to define the desired final structures. Because there are two spacers for each mandrel, the feature density is doubled.

As widely addressed in Section 2.1.2, relevant areal densities for potential BPM products begin above 1.5 Tb/in^2 which translates to lithographic islands having a critical dimension (CD) < 10 nm with a full pitch <20 nm. Because sub-10 nm lithography is not available by any conventional lithographic technique, block copolymer lithography has evolved as an organic part of the BPM patterning solution not only because of the ability of BCPs to form sub-lithographic features, but because of their flexibility to comply with other important BPM design requirements such as conforming to zoned periodic features on circular tracks at constant angular pitch.

There are currently two alternatives to stretch to the sub-20 nm space. 1) By using a high χ block copolymer material it is possible to achieve a full pitch even below 10 nm (see Section 1.4.1).[45, 46] However, potential solutions with high χ BCPs are still developing and will require additional innovations to overcome current challenges in controlling interfacial energies, DSA and pattern transfer. 2) By contrast, an extension of the well-known spacer defined double patterning (SDDP) can be readily applied to block copolymer lithography to further subdivide the pitch obtained by PS-b-PMMA block copolymers. In principle, this provides a path to reach 11 nm full pitch with currently available PS-b-PMMA BCPs. However, SDDP for sub-20nm pitch is a complex solution with multiple challenges in dimension control, spacer deposition, and materials design. It is worth noting that with SDDP, currently available materials and methods can reach to >3 Tb/in^2 by further optimizing currently available processes.

In Chapter 3, we demonstrate a scalable process to fabricate nanoimprint templates with critical dimensions of 7.5 nm.[133] To achieve this feature size we combine directed self-assembly (DSA) of block copolymer (BCP) and spacer defined double patterning. Spacer defined double patterning for BPM was previously addressed in literature[134] but this is the first account of the nanofabrication process details. In Chapter 3, we focus on optimization of the selective infiltration of aluminum oxide to define a 30 nm pitch hard mask derived from a BCP pattern. In addition, we studied the ALD process used to create the double patterned features. We investigate the growth of two different materials, SiO_2 and TiO_2 on relevant materials using spectroscopic ellipsometry and SEM. We find that depending on the precursor reactivity, some plasma processes are incompatible with the carbon such that it is etched by the plasma oxidation steps during deposition. Ultimately, we demonstrate 7.5 nm TiO_2 half-pitch features can be patterned with a proper combination of etching and thermal assisted ALD. While we study the process for application in BPM, the process is useful for imprint template fabrication in general.

Chapter 3

Atomic Layer Deposition for Spacer Defined Double Patterning of sub-10 nm Titanium Dioxide Features

Overview

The next generation of hard disk drive technology for data storage densities beyond 5Tb/in^2 will require single-bit patterning of features with sub-10nm dimensions by nanoimprint lithography. To address this challenge master templates are fabricated using pattern multiplication with atomic layer deposition. Sub-10 nm lithography requires a solid understanding of materials and their interactions. This chapter focuses on the spacer defined double patterning technique, which is capable of producing a pattern two times as dense as the original. Silicon dioxide and titanium dioxide are introduced as pattern spacer materials and their interaction to carbon, chromium and silicon dioxide are studied. Thermal titanium dioxide atomic layer deposition allows for conformal deposition of a spacer layer without damaging the carbon mandrel and eliminates the surface modification due to the reactivity of the metalorganic precursor. Finally, using self-assembled block copolymer lithography and thermal titanium dioxide spacer fabrication, pattern doubling with 7.5nm half-pitch spacer features is demonstrated.

3.1 Spacer Defined Double Pattering for Bit Patterned Media

The future of magnetic data storage beyond perpendicular recording will require replacing the conventional granular magnetic media with bit patterned media (BPM).[135, 136] Lithographically defining the single bit is necessary to maintain the thermal stability needed for magnetic recording.[137] In order to reach storage density beyond 5Tb/in^2, BPM demands isolated sub-10 nm feature sizes over a large area.[138]

Current optical lithographies do not have the resolution to meet the critical dimension requirements.[139] Electron beam lithography has sub-10 nm resolution,[140] but is a serial method with low-throughput.[141] Cross-Nanoimprint lithography (NIL) [71, 135] on the other hand, allows for stitchless, high volume production and enables to pattern features at the single-digit nanoscale.[142, 143] As UV curing is preferred over thermal curing [71, 135], the master template is usually fabricated from quartz substrates. Herein, we target fabricating master templates on quartz to meet BPM with an areal density greater than 5Tb/in^2. This requires sub-10 nm half-pitch features to be patterned with single nanometer control. For these reasons a solid understanding of the deposition process and etch properties of suitable materials for UV-NIL template fabrication is required in order to maintain critical dimensions.[1, 3, 14, 134]

Double patterning methods have been adopted in the interim [144, 145] to overcome resolution limitations by halving feature size and pitch.[146-148] Among the different double patterning techniques, Spacer Defined Double Patterning (SDDP) gains particular attention because it does not suffer from overlay issues and can achieve high throughputs.[149, 150] In SDDP (Figure 3.1, progressing from steps (d) to (f)), a highly conformal spacer layer is deposited onto a sacrificial mandrel pattern. Next, the spacer is etched back and the mandrel removed, resulting in a patterned layer with narrow spacer features. The key element for a successful SDDP integration is the performance of the spacer technology. Atomic Layer Deposition (ALD) is particularly appropriate for the spacer fabrication[151, 152] because it produces excellent conformity and uniformity without loading effect across an entire wafer.[150] Loading is the decrease of deposition rate with an increase in the amount of exposed material being deposited. ALD allows the formation of ultra-thin films with angstrom-level resolution by cyclical oxidation of a metalorganic precursor.[153, 154] Control of the ALD parameters is instrumental in defining the feature size and frequency of the double patterned lines.

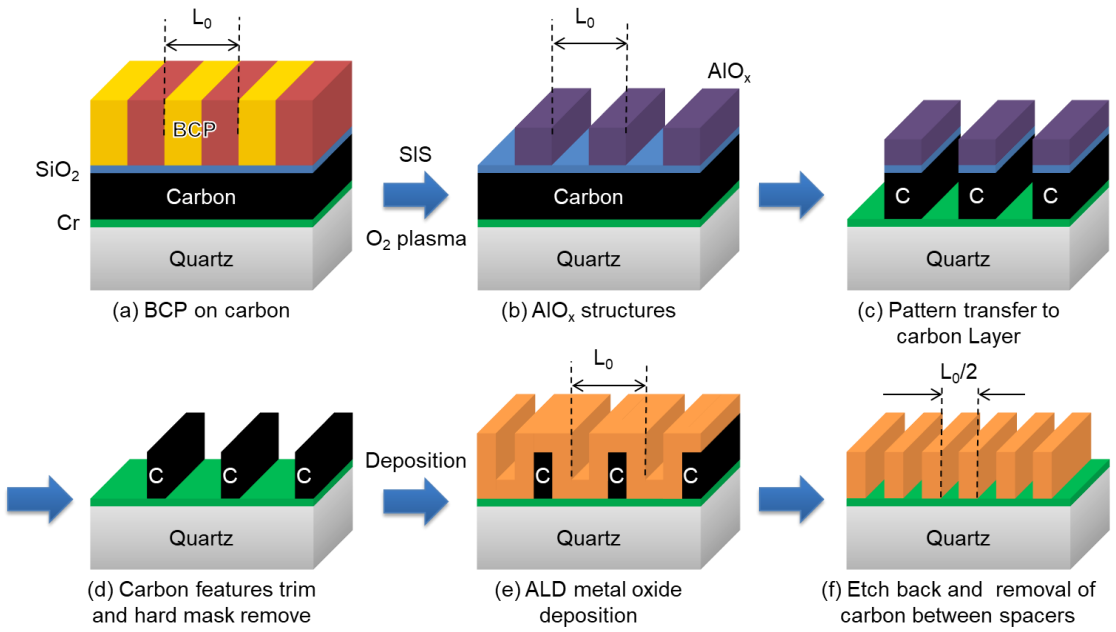

Figure 3.1 Line frequency doubling flow. (a) Initial PS-*b*-PMMA BCP pattern. (b) Sequential Infiltration Synthesis (SIS) of Al_xO_y using atomic layer deposition and polymer removal treatment to release lithographic nanostructures. (c) Pattern transfer to SiO_2 hardmask and sacrificial carbon layer etching. (d) Carbon line trimming and SiO_2 hard mask stripping. (e) Conformal Titanium Dioxide spacer deposition using ALD. (f) Spacer etch back and strip of sacrificial carbon between spacers.

The ALD deposition step in SDDP must fulfill three main requirements for achieving single-digit nanometer accuracy. First, the oxide deposition must not damage the underlying materials. Second, nucleation and growth on different surfaces should promote the formation of either a uniformly thick film or a thinner film at the bottom of the trenches. An uneven film with less deposition at the bottom of the trench would balance the discrepancy in the etching rate between trench tops and bottoms (tops tend to etch faster than bottoms).[155] Finally, the deposited material should have enough mechanical integrity to prevent line collapse when the mandrel is removed.

This Chapter focuses on the atomic layer deposition process used during SDDP. The ALD layer grows on two different materials: carbon, which defines the mandrel, and chromium, which defines the hard mask for future quartz etching (Figure 3.1(e)). To begin this study we prepared flat substrates of carbon, chromium as well as silicon dioxide, which is used as a reference material. Using flat samples is imperative for the *in-situ* spectroscopic ellipsometry (SE) to study the growth of the ALD layers (section 1.5.1). During the ALD of titanium dioxide (TiO_2) and silicon dioxide (SiO_2), we look at nucleation and etch properties to

better understand the initial deposition phase. We show that the plasma processes using tris(dimethylamino)silane (TDMAS) as the SiO_2 precursor interacts with the carbon. TiO_2 worked with both plasma and thermal processes. However, thermal processes better maintained the integrity of the underlying carbon and chromium layer.

After defining a viable spacer deposition process with blanket samples, our patterning approach employs the use of self-assembled block copolymer lithography [156] in combination with spacer defined double patterning [147] to reach the sub-10 nm regime (Figure 3.1). Patel *et al.* demonstrated the use of multi-patterning for pitch doubling from a starting lamellae polystyrene-*b*-poly(methyl methacrylate) (PS-*b*-PMMA).[157] Here we use PS-*b*-PMMA with 30nm starting pitch. From previous research, we demonstrated nanoscale etching of relevant materials for imprint template fabrication at sub-10 nm dimensions.[89, 158-161] We build on this experience to identify a material stack with coordinated selectivities for high resolution pattern transfer in the SDDP process. By using the results of the ALD study, we ultimately show the fabrication of ALD generated TiO_2 features on chromium with 7.5nm width.

3.2 SDDP Fabrication and Characterization

In this Chapter, two types of substrates were used: (1) flat substrates for ellipsometric analysis and (2) patterned structures for sub-10 nm features fabrication.

3.2.1 Flat substrates fabrication (1)

SiO_2 and TiO_2 were grown in a plasma-enhanced ALD reactor (Oxford Instruments FlexAL) on three types of flat substrates; thermal silicon dioxide (SiO_2), e-beam evaporated chromium (Cr) and sputtered carbon (spC). Carbon and chromium coated wafers were used to represent the carbon mandrel and chromium underlayer respectively, while SiO_2 was used as a reference material. Temperatures of 200˚C and 300˚C were used because these higher temperatures promote mechanical strength and reduce collapse after removing the mandrel[148, 162, 140, 155].

Nucleation and growth during atomic layer deposition were studied *in-situ* using spectroscopic ellipsometry (J A Woollam Co., Inc., M2000) fitted on the Oxford FlexAL ALD reactor. Under many conditions, SE can detect thickness changes in the submonolayer range.[78] Substrates were measured before ALD deposition to facilitate the optical modeling

of the material film during growth. The optical constant of the ALD material was determined after 200 cycles and then used for modeling the film thickness.

3.2.2 Spacer defined pattern doubling for sub-10 nm features (2)

The process we considered for BPM master template fabrication is shown in Figure 3.1. The process in total involves 6 dry etching steps, 1 wet etching step, and 2 deposition steps. All the steps involved in the SDDP have been properly developed in order to have stable and reproducible results and minimize time-to-time variations. Samples of 1 x 1 in^2 were used during the optimization of the processes. Over these samples, the features were completely uniform.

Material stack: The material stack (provided by Seagate Technology LLC) is comprised of a 6" prime grade silicon wafer substrate with 300 nm thermal SiO_2, 5nm e-beam evaporated chromium, 20nm sputtered carbon and a 7nm SiO_2 layer. The unguided block copolymer film of PS-*b*-PMMA block copolymer had a full pitch of 30nm.

Figure 3.1(a) → Figure 3.1(b): *Sequential Infiltration Synthesis (SIS):* In order to enhance the selectivity between the pattern formed by BCP and the underlying SiO_2, aluminum oxide was selectively synthesized in the PMMA domain by exposing the PS-*b*-PMMA film to TMA and water vapors [154, 163-167]. The infiltration was performed using an Ultratech/Cambridge NanoTech Savannah (S100) ALD system. The process temperature of 85˚C, is below the glass transition temperature of PS-*b*-PMMA BCP [168]. The precursors exposure was carried out at a pressure of 250mTorr with a dosing time of 300 seconds.

Polymer removal: After selectively hardening the PMMA domain over PS, the BCP film was stripped by oxygen plasma in an Oxford Instruments 80+ Reactive Ion Etcher (RIE) at 110 V DC bias and 20˚C to remove the remaining polymer and form infiltrated Al_xO_y lines (Figure 3.1(b)).

(b) → (c): *Pattern transfer to SiO_2:* A 7nm SiO_2 layer is used under the BCP to promote a specific surface chemistry for graphoepitaxy.[156] The Al_xO_y lines are transferred to this SiO_2 layer using fluorine-based plasma. The etching was carried out in a multiple frequencies parallel plate tool (Oxford Instruments) with 60 MHz on the top plate and 13.56 MHz on the bottom plate. The chamber was filled with 80 sccm SF_6 at 20% O_2 and kept at 5mTorr. We

applied 150 W of radio frequency power and 400 W VHF forward power for 6 s. The resulting SiO_2 lines were used as a hard mask for etching the 20nm sputtered carbon layer.

Carbon etch and trim: The Carbon was etched in an oxygen plasma at cryogenic temperature (-100˚C) in an Oxford Instruments PlasmaLab 100 (Cobra) Inductively Coupled Plasma (ICP) system. The forward power was 20 W and ICP power was 1000 W. The flow rate of O_2 was 20 sccm, and chamber pressure was set to 6mTorr (Figure 3.1(c)). The width of the lines was controlled by the etching time. A 90 s etch time left a 15nm line. Increasing the etching time to 270 s reduced the mandrel width to 8nm.

(c) → (d): *Hard mask stripping:* SiO_2 and Al_xO_y were removed by hydrofluoric acid dip (40% dilution) leaving carbon lines at 30nm pitch and 8nm width (Figure 3.1(d)).

(d) → (e): *Titanium Dioxide deposition:* 7.5nm thick TiO_2 film was conformally deposited on trimmed mandrel lines by thermal atomic layer deposition (Oxford FlexAl) at 200˚C. The process used alternating steps of Tetrakis(dimethylamido)titanium (TDMAT) dosing and oxidation in which reactive oxygen was created from water vapor. TDMAT dosing was carried out at a pressure of 80mTorr for a time of 800ms, followed by a 6 s purging step. The oxidation step was then performed using water vapor at a pressure of 80mTorr for 120ms. The water dose was followed by 10s purging step with 400sccm argon gas flow.

(e) → (f): *Etch back:* The planar surfaces on the bottom and the top of the deposited TiO_2 were etched back in a fluorine-based ICP-RIE. At 4mTorr the flow rates CF_4 and O_2 were 33sccm and 3sccm respectively. Etching was done for 45s at 25W RF power and 180W ICP power. After etching, the height of the features was reduced to 8nm.

Carbon strip: The carbon mandrel was removed by O_2 plasma at 20˚C in an ICP-RIE at low forward power of 2W RF with 1V DC bias to prevent damage to the TiO_2 lines. Process conditions had an oxygen flow of 8sccm, pressure 5mTorr, ICP power of 250W and 75s etch time.

3.3 Atomic Layer Deposition enables SDDP

3.3.1 SIS and PS removal to define a 15nm half-pitch lithographic pattern

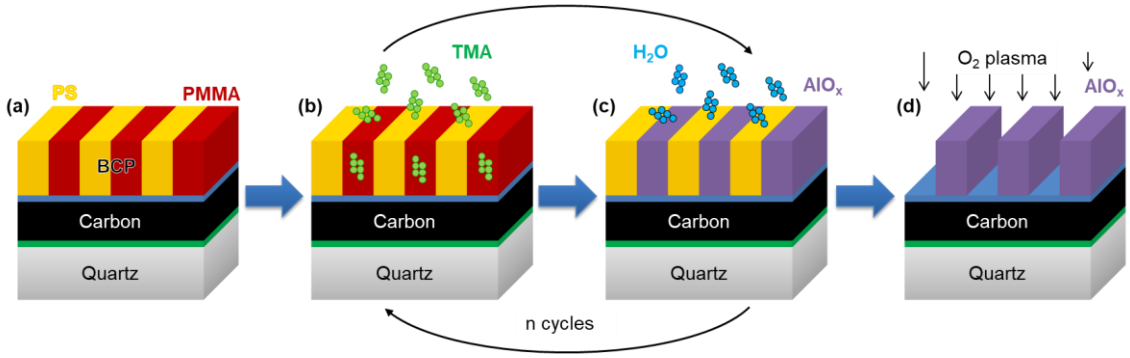

Figure 3.2 Schematic cross-sectional view of the Sequential Infiltration Synthesis (SIS) process flow. (a) Self-assembled PS-b-PMMA BCP. Repeating (b) TMA and (c) water vapor precursor exposures form alumina within PMMA domains. (d) Polymer removal by O_2 plasma.

The goal of this step is to create a hardmask from the original BCP pattern that has the appropriate dimension ($L_0/2$, the BCP half-pitch). Polystyrene (PS) and poly(methyl methacrylate) (PMMA) typically have limited etching selectivity in plasma processes. Indeed, PMMA can be removed and leave a residual PS pattern but the low etching contrast means that typically there is some damage and loss of critical dimension to the polystyrene.[169] Peng *et al* demonstrated polymer infiltration with Trimethylaluminium (TMA, $Al(CH_3)_3$) gas using an atomic layer deposition tool as a way to increase etching contrast between the polymer blocks.[168, 170] In sequential infiltration synthesis (SIS), a polystyrene-*b*-poly(methyl methacrylate) PS-*b*-PMMA film is exposed to TMA vapor precursor inside an ALD reactor (Figure 3.2(b)). The vapor diffuses inside the polymer and selectively binds to carbonyl groups in PMMA.[163, 165] The excess precursor vapor is pumped away and water vapor is introduced to finish the reaction forming aluminum oxide only where the PMMA was located (Figure 3.2(c)). The full cycle is repeated to increase the amount of deposited material. A subsequent oxygen plasma treatment removes the polymer matrix and densifies the aluminum oxide pattern that resembles that of the original block copolymer pattern which can be used as an etch mask to transfer the pattern into the substrate (Figure 3.2(d)). SIS has been found to have the benefit of reducing line-edge-roughness of the BCP pattern.[134] Here we address the challenge of finding the window where the infiltration reaction occurs only within one block and produces features of the correct width.

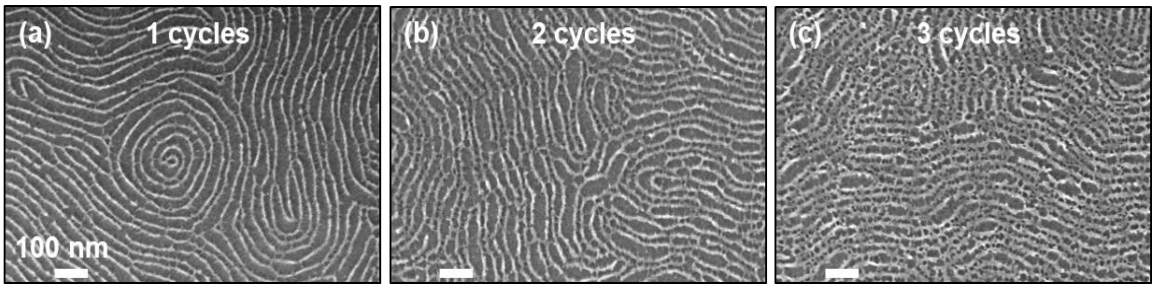

Figure 3.3 Top-down SEM images of 30nm pitch self-assembled PS-PMMA lamellar pattern infiltrated with alumina. (a) to (c) remaining alumina pattern formed using 1, 2 and 3 cycles after oxygen plasma removal of organic material. ALD pressure during SIS was fixed at 200mTorr.

Process pressure plays a strong role in the infiltration because it is directly proportional to the precursor diffusion inside the polymer. We studied pressures of 2.5 Torr and 0.20 Torr at infiltration times of 300 s. We first tested the low pressures to evaluate the feasibility of using our existing ALD reactor for SIS, an Oxford Instruments FlexAL ALD with maximum pressure of 200mTorr.

Figure 3.3 shows the results of SIS performed at 200mTorr for the entire process. The substrate temperature is fixed at 85˚C in order to keep the diblock copolymer below its glass transition temperature and the PS/PMMA domains segregated during SIS. After the infiltration process, PS and other organic residues were removed by 180s oxygen plasma RIE (80mTorr, 50sccm O_2, 20 W (DC bias = 110V).

After one SIS cycle (Figure 3.3(a)) the resulting Al_xO_y line width is less than a third of the original one. Moreover, lines are not continuous and are subject to pitch walking. Al_xO_y is also detected in the spaces between the lines. This effect increases with the number of cycles and after three SIS cycles the aluminum oxide covered the surface completely (Figure 3.3(c)). Low pressure prevents the precursors to diffuse inside the BCP; TMA and Water react on the BCP surface. During the first cycle, TMA reacts with the most external carbonyl group of PMMA and oxidizes in aluminum oxide when water vapor is inserted into the chamber. In the following cycles, Al_xO_y nucleates from the seed created during the first cycle, mainly on the BCP external surface. This was consistent with the findings of Ramanathan *et al.*[168]

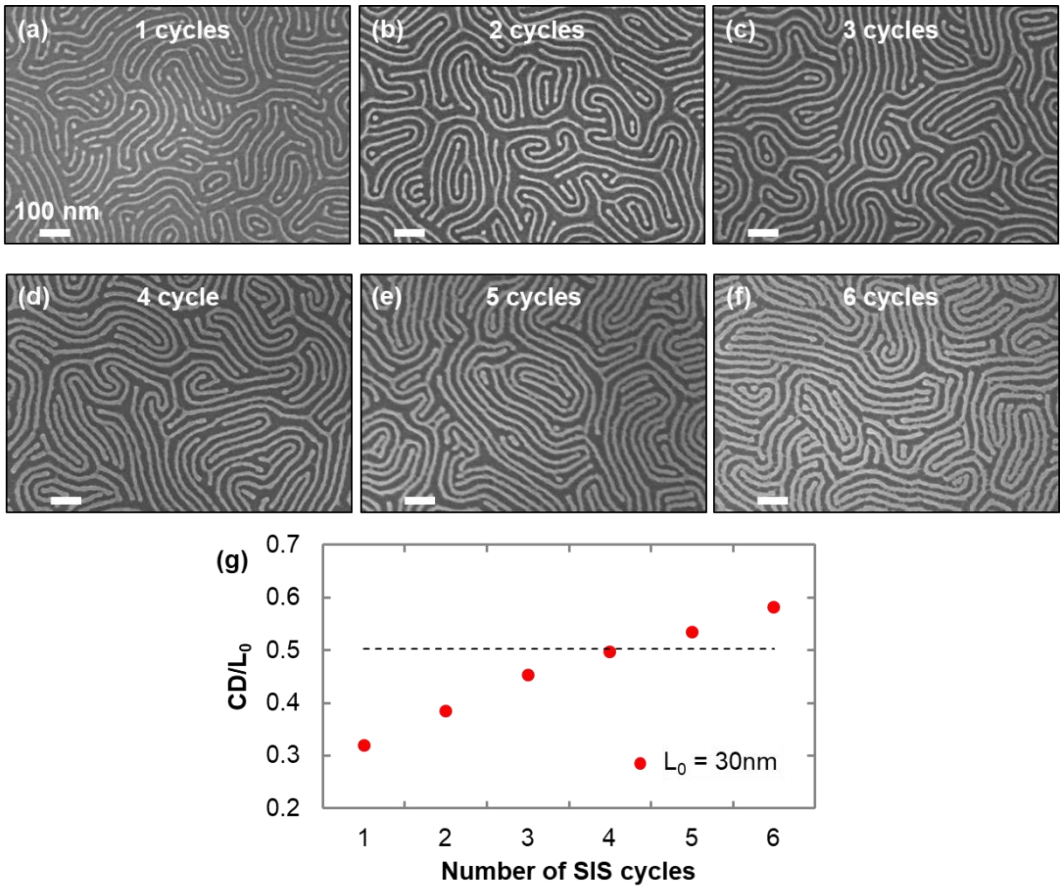

Figure 3.4 (a)-(f) Top-down SEM images of PS-b-PMMA films infiltrated with alumina at 2.5 Torr using 1 to 6 TMA/water cycles after O_2 plasma removal of organic material. (g) Plot of pattern CD (in units of L_0 = 30nm) vs. number of TMA/water infiltration cycles. Dashed line represents the critical dimension of the initial polymer pattern.

We moved to an Ultratech/Cambridge NanoTech ALD reactor which was capable of higher process pressures and allowed to create a final pattern of the appropriate dimensions. Figure 3.4(a)-(e) show top view SEM pictures of unguided lamellae PS-*b*-PMMA with 30nm pitch after SIS using 1 to 6 TMA/water cycles and subsequent polymer removal by oxygen plasma. After one TMA/water cycle (Figure 3.4(a)) the alumina lines show some discontinuities, but after four cycles (Figure 3.4(d)) the lines are continuous. Further increasing the number of exposure cycles causes the infiltrated lines to be rougher; also Al_xO_y is detected between the lines. The size of the final features depends on the number of SIS cycles (Figure 3.4(g)). The first infiltration cycle creates features with a CD/L_0 ratio of 0.32. This CD/L_0 ratio increases approximately linearly over our process window at a rate of 0.05 per cycle. The dashed line represents the 0.50 width ratio of the original PS-*b*-PMMA

BCP template and constitutes the targeted CD after SIS. After four SIS cycles (Figure 3.4(d)) we obtained lines with CD = 0.49 L_0 which are an excellent representation of the original BCP pattern. This pattern was transferred into the underlying SiO_2 layer using. The resulting lines were then used as a hardmask to transfer the pattern and carefully trim the underlying carbon layer. The carbon layer then acted as the mandrel for spacer defined double patterning using the atomic layer deposition.

3.3.2 ALD growth on flat substrates

Silicon dioxide deposition was tested both thermally and with plasma on flat substrates (1), using tris(dimethylamino)silane (TDMAS) as a precursor. However, surface species deposited by TDMAS were found to be unreactive using water vapor at temperatures ranging from 40–300 ˚C. After 200 cycles of thermal SiO_2 ALD, no material was detected on the surface by in-situ SE analysis. This result is consistent with the previous finding of Burton and Kang.[171] SE measurements show SiO_2 thin films deposits from TDMAS and O_2 plasma at 300˚C on silicon dioxide and chromium with a growth rate of 0.036±0.005 nm/cycle (Figure 3.5(a)). The initial growth rate of SiO_2 on chromium is higher than SiO_2 on SiO_2 due to the formation of chromium oxide which results in an apparent increase in thickness. Notably, plasma SiO_2 deposition on sputtered carbon produced unexpected results. After 100 cycles SiO_2 plasma-enhanced ALD, the carbon layer was no longer present (Figure 3.5(b) – TDMAS – O_2 plasma ALD). We initially hypothesized that the plasma etching step removed the carbon. However, we found that running a continuous oxygen plasma step with the same process condition used in ALD oxygen step (Figure 3.5(b) – O_2 plasma only) produced a carbon etch rate much lower than the etch rates we observed during the full ALD sequence. The ALD precursor exposure step run alone was not found to remove any carbon (Figure 3.5(b) – TDMAS only). Presumably, there is a synergistic reaction between the SiO_2 precursor and carbon that promotes faster removal in an oxygen plasma. Overall we did not find a suitable thermal or plasma ALD process using the TDMAS precursor for deposition of SiO_2. We subsequently found success investigating the TiO_2 ALD process.

Titanium oxide ALD films were deposited from Tetrakis(dimethylamido)titanium (TDMAT) metal-organic precursor on sample type (1) using both thermal and plasma processes. To minimize line edge roughness due to crystallinity, we performed TiO_2 growth at temperatures below 250˚C where the formation of large crystallites is minimized [37, 172, 173].

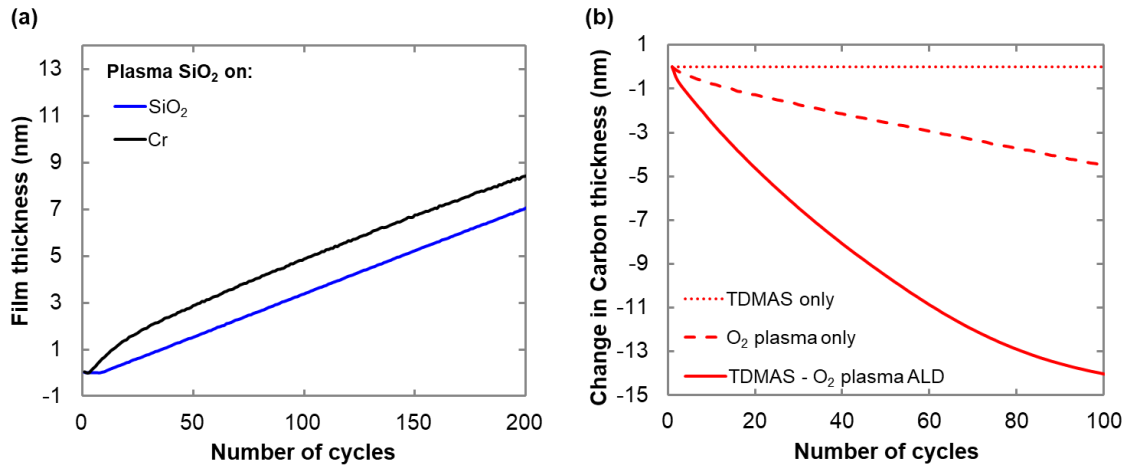

Figure 3.5 (a) ALD growth of plasma SiO_2 at 300˚C on two substrates: thermal SiO_2 and Chromium (Cr). (b) Changes in carbon thickness during plasma SiO_2 ALD deposition at 300˚C (continuous line), O_2 plasma exposure step alone (dashed line), and TDMAS injection step alone (dotted line).

Unlike our SiO_2 precursor, TDMAT works in both thermal and plasma-based processes and we were thus able to evaluate both. Figure 3.6(a) shows the nucleation behavior of thermal and plasma TiO_2 ALD at 200˚C on the three different substrates: chromium, carbon, and silicon dioxide. Nucleation behavior of the films on these substrates is shown in Figure 3.6(b). While the growth rates of thermal and plasma ALD are not significantly different, 0.042±0.005 nm/cycle for thermal vs. 0.052±0.005 nm/cycle for plasma, the nucleation behavior is different. As observed in the plasma growth of SiO_2 on chromium, the nucleation of TiO_2 shows a higher slope. This behavior is absent in the thermal growth. We hypothesized that oxygen plasma promotes an apparent change in thickness due to the formation of chromium oxide. This conclusion is confirmed in the work of Langereis *et al.*[37] where they show an initial accelerated growth during plasma ALD on different substrates. When plasma TiO_2 grows on carbon, measured film thickness first drops below zero and then increases to reach a constant growth rate. We believe the carbon is etched during the nucleation phase, the first few cycles, and then the carbon surface is passivated with the first layers of TiO_2. Note, however, that when carbon is used as a mandrel in the patterning process, any etching can be detrimental for sub-10 nanometer dimensions. Therefore, in order to minimize damage to the substrate and to avoid any etching, oxidation or acceleration during the growth, we decided to move away from any O_2 plasma activated process.

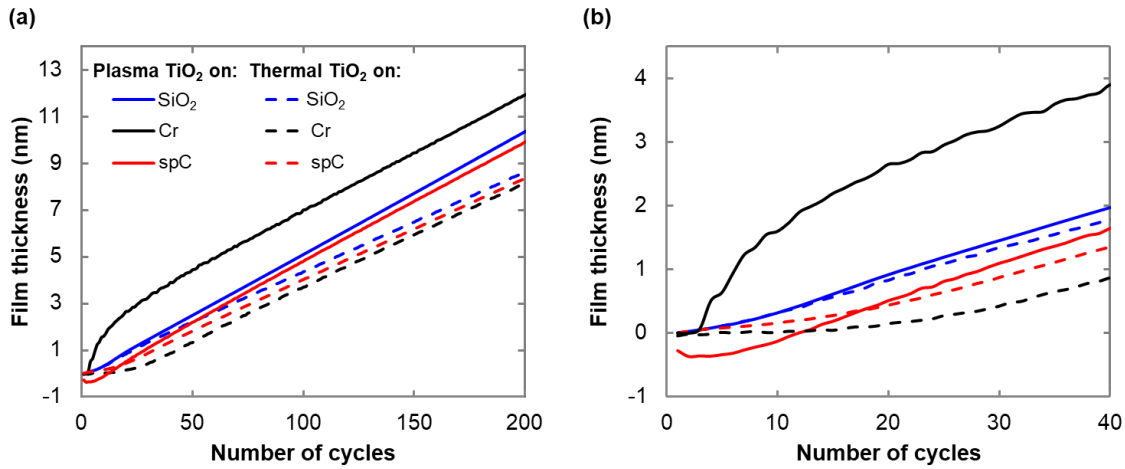

Figure 3.6 (a) TiO_2 layer thickness measured by in-situ SE as a function of the number of ALD cycles at 200˚C on different substrates: thermal silicon oxide (SiO_2 - blue), carbon (spC - red), chromium (Cr - black). Titanium dioxide ALD alternated TDMAT dosing and oxidation where oxygen is given by water vapor (dashed line) and O_2 plasma (continuous line). Graph (b) represents a zoom of the first 40 cycles of the deposition, showing the nucleation behavior.

Nucleation of thermal TiO_2 on the three substrates does not show any etching, and a delay is observed on chromium. This delay is small and unlikely to result in a significant process benefit (reduced ALD thickness at the trench bottoms to counteract reduced etch rates) [155]. Overall, the TiO_2 thermal process was the best process identified and used as the ALD step in our SDDP process.

3.3.3 Demonstration of 7.5nm half-pitch TiO_2 features via SDDP

Figure 3.7 shows selected key steps of the full pattern doubling process in a top down view. The selective infiltration process was optimized to create an initial pattern of 15nm (PS-*b*-PMMA half-pitch) after infiltration and polymer removal (Figure 3.7(b)). This pattern is etched into the oxide layer and then the carbon (Figure 3.7(c)). After the carbon trim step and mask removal, Figure 3.7(d) shows an increase in edge roughness in the top down image. However, we found that subsequent process seemed to smooth the sidewalls. Next, TiO_2 was deposited by atomic layer deposition, using the thermal deposition process at 200˚C. This ALD layer was etched to produce titanium features at 7.5nm half-pitch (Figure 3.7(e)).

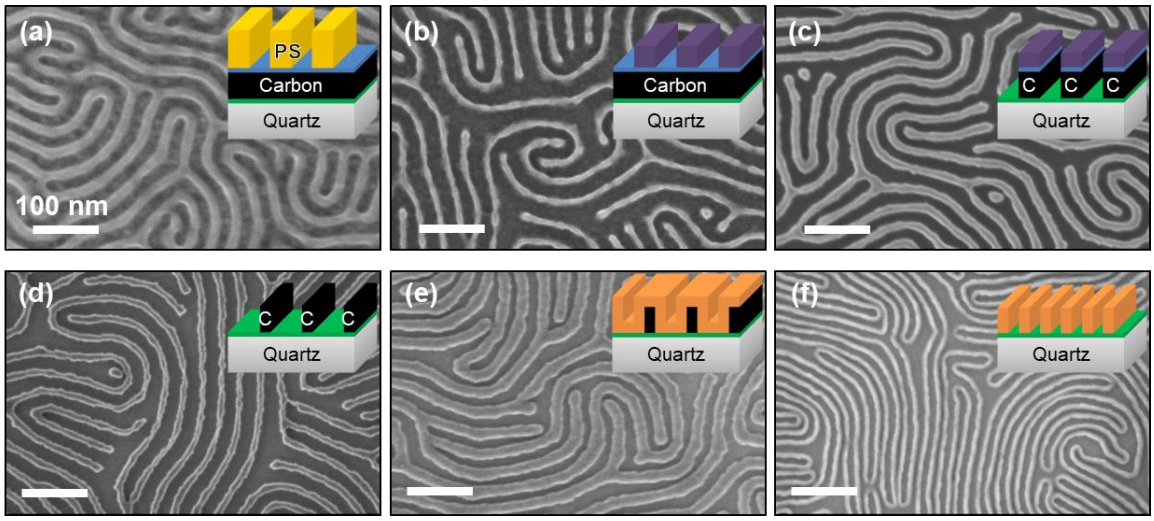

Figure 3.7 Top view SEM images of unguided BCP line doubling pattern transfer demonstration corresponding to the schematic process flow in the inset. (a) Self-assembly of PS-*b*-PMMA BCP with 30nm pitch after stripping the PMMA. (b) Pattern after selective sequential infiltration synthesis of Al_xO_y in the PMMA domain and polymer removal. (c) Pattern transferred to SiO_2 and carbon mandrel. (d) 30nm pitch, 7.5nm wide carbon mandrel lines. (e) Conformal thermal ALD of TiO_2 spacer over mandrel features. (f) 15nm pitch spacer lines after etching and mandrel removal.

Figure 3.8 shows a cross-sectional view of the last three steps in the double patterning process. Figure 3.8(a) shows 30nm pitch carbon mandrel lines fabricated using PS-*b*-PMMA block copolymer along with SIS pattern transfer. Figure 3.8(b) shows the resulting 7.5nm conformal TiO_2 spacer deposited on the carbon mandrel. After back etching the TiO_2 using CF_4 at 10% O_2 in an inductively coupled plasma reactor, Figure 3.8(c) shows resulting features with 7.5nm half-pitch. ICP power of 180 W and RF of 25 W etch 7.5nm TiO_2 in 30 s. In order to etch through TiO_2 at the bottom of the trenches, a longer etching time is used. This leaves TiO_2 features with a height of 8nm (after mandrel removal using standard oxygen plasma) (Figure 3.8(c)). TiO_2 is a high selectivity mask for the subsequent chromium patterning step so this height is sufficient to pattern the underlying chromium. Note, that some lines in Figure 3.8(c) appear tilted. This is not due to pattern collapse but rather an artifact of the conformal coating of the carbon mandrel. During the oxygen etching and trimming of carbon features, carbon structures develop a widened footing portion at their base (Figure 3.8(a)). After etching the TiO_2 layer, the remaining feature conforms to the tilt of the carbon pattern. The TiO_2 structures in Figure 3.8(c) could be used directly as the structural template material, or alternatively transferred to the underlying chromium layer using chlorine and oxygen gas mixture plasma.[89]

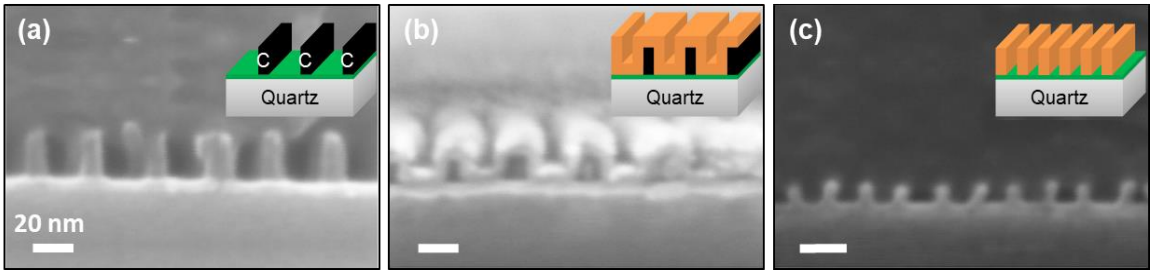

Figure 3.8 (a), (b) and (c) Cross-sectional view SEM images of the double patterning steps corresponding to the schematic in the top right corner. (a) 30nm pitch sputtered carbon mandrel lines. (b) Conformal thermal ALD TiO_2 spacer deposition over 8nm carbon mandrel features. (c) 7.5nm pitch TiO_2 lines after SDDP.

3.4 Conclusion

We were able to fabricate sub-10nm half-pitch pattern through a combination of self-assembled block copolymer and spacer defined double patterning. Chapter 3 demonstrates the fabrication of 15nm carbon lines using selective infiltration by atomic layer deposition of PS-*b*-PMMA block polymer. Using spectroscopic ellipsometry, we conducted detailed studies of the deposition of the spacer on flat substrates, chromium and carbon, as a function of the number of ALD cycles. After studying SiO_2 and TiO_2 processes, both plasma and thermal, we chose a thermal TiO_2 process. SiO_2 could only be deposited by plasma and ended up etching the carbon. We demonstrated the etching process was due to a synergistic reaction between the ALD precursor and the O_2 plasma; O_2 plasma alone etched the carbon considerably slower. Carbon was more stable in the TiO_2 plasma process but underwent some etching. In addition, it appeared that plasma processes promoted the growth of chromium oxide. We thus moved to a thermal TiO_2 process for SDDP demonstration which did not damage the mandrel and ends with 7.5nm robust standing lines that are not subject to pattern collapse. However, the lines did exhibit a slight tilt. To minimize this tilt, the carbon trim will need to be optimized to reducing any footing at the bottom of the feature.

Overall, using spacer defined double patterning fabrication approach we proposed a systematic route to enable sub-10nm feature size transfer over large areas. Notably, it is possible to take advantage of the wafer stack and extend the implementation of this method using substrates compatible to chromium deposition. This type of process enables scalable fabrication of single digit nanometer feature sizes for both patterned media at

densities beyond 5 Tb/in^2 and integrated circuits. The next steps in BPM master template fabrication are to transfer the TiO_2 pattern into the underlying chromium and then into the quartz template. This will be demonstrated in subsequent work.

Chapter 4

Plasma generation for material etching

Overview

In this section, we will discuss the most commonly utilized plasma reactor types in integrated circuits (ICs) manufacturing, revealing their merits and drawbacks. With special attention to SiO_2 etching, the mechanism for conventional etching is reported. Limitations rising in pattern transfer using plasma processing are explained and atomic layer etching (ALE) is then introduced. Fluorocarbon based atomic layer etching for SiO_2 patterning overcomes limits of conventional etching.

4.1 Plasma etching

Chemically reactive plasma discharges are widely utilized to modify the surface properties of materials.[174] Nowadays, it is impossible to imagine global manufacturing on the scale we see without plasma processing technology. In particular, this material processing technique plays a crucial role in the fabrication of modern (nanometer scale) semiconductor devices as well as for manufacturing the very large scale integrated circuits. Some technological steps (etching, deposition, doping) are repeated many times during the IC manufacturing. Since one third of the tens to hundreds of fabrication steps in IC manufacturing are plasma based,[174] plasma processing technology is unavoidable for the entire electronics industry.

Typical plasmas which are used to this end are low pressure discharge, being generated in vacuum within a plasma processing reactor. Generally, the plasma sources for technological operations like etching or deposition consist of a vacuum reactor chamber with grounded sidewalls, where the process gases are introduced into the chamber through a special inlet. Not only plasma chemistry arises in the reactor, but also the kinetic energy of the ions bombarding the target surface plays a crucial role. For example, the threshold energy for ion-enhanced etching of silicon oxide with Ar^+ ions is 40 eV.[175] Therefore, in the reactor the substrate to be processed is placed on the cathode, which has a negative floating potential with respect to the plasma, forcing acceleration of the positively charged ions towards the bottom electrode. Since, in many cases, the floating potential at the cathode is not enough to provide sufficient ion energies for sputtering processes, the cathode is driven by an RF power source via a blocking capacitor, which suppresses the DC current. Hence, during each positive half cycle the electrons reach the sample and discharge it, allowing a much larger potential drop between the plasma and the electrode. Due to the various physical phenomena inside the reactor, (recombination, diffusion out of the plasma bulk, or adsorption and/or neutralization at the reactor sidewalls), the number of charge carriers in a plasma decreases with time. In order to sustain the plasma, the loss of charge carriers must be compensated for. Therefore, additional energy should be constantly coupled into the discharge. This additional energy supply results in an increase in the ion and electron temperatures and gives rise to ionization processes within the plasma bulk. In an inductively coupled plasma (ICP) process, the energy is inductively coupled into the plasma.[176]

4.2 Inductively coupled plasma (ICP)

In order to satisfy the criteria of damage, selectivity and linewidth control for the next-generation ICs fabrication, it should be possible to control the ion bombardment energy together with its energy distribution independently of the ion and neutral fluxes. The need for large area, high-density plasma sources for plasma-aided manufacturing of integrated circuits has led to a renewed interest in inductively coupled plasmas (ICPs). Main merits of ICP sources are as follows:[177]

- high densities of ions, electrons and radicals,
- excellent uniformity over diameters of at least 20 cm,

- low and controllable ion energies,
- negligible contamination from reactor sputtering or particulate generation.

In inductively coupled plasma etchers, plasma is generated by a source that is inductively coupled to the plasma. The ion-density in these etchers is generally about an order of magnitude or more higher than in the other etchers.[178] The wafer is placed on an RF biased lower electrode, and plasma is generated by a source placed a short distance above the wafer. In an ICP system, a coil outside the chamber is used for plasma generation (ICP power). As a result, the source is decoupled from power delivered to the stage to allow ion-energy control independent of plasma density.

The ICP plasma is generated and sustained by the application of RF power (typically 13.56 MHz) to a non-resonant inductive coil, which is usually located outside the reactor, around its chamber. As a result, a strong time-varying magnetic field appears inside the ICP reactor chamber, which in turn, by means of induction, gives rise to an electric field inside the chamber, that causes ionization of the process gases.

The described non-capacitive power transfer is the key to achieving low voltages across all plasma sheaths: at the cathode as well as at the surfaces of the reactor walls. The DC plasma potential, and hence the ion acceleration energy, is then typically 20-40V.[179] The electrode on which the substrate is placed (the cathode), is driven by a capacitively coupled RF source, thus enabling an independent control of the ion bombarding energy, whereas the ion/radical fluxes are controlled by means of the ICP source power.

Due to the aforementioned characteristics, ICP etching systems are routinely employed in industry for the fabrication of integrated circuits and nanofabrication.[180] In the majority of cases, typical ICP processes have pressure values in the range of 1-100 mTorr. Among the most common ICP-driven processes are the following:

- anisotropic dry silicon etching with high etching rates
- etching of III-V-semiconductors with a low damage to the crystal structure
- etching of silicon dioxide SiO_2 with high etching rates
- gold and platinum sputter etching

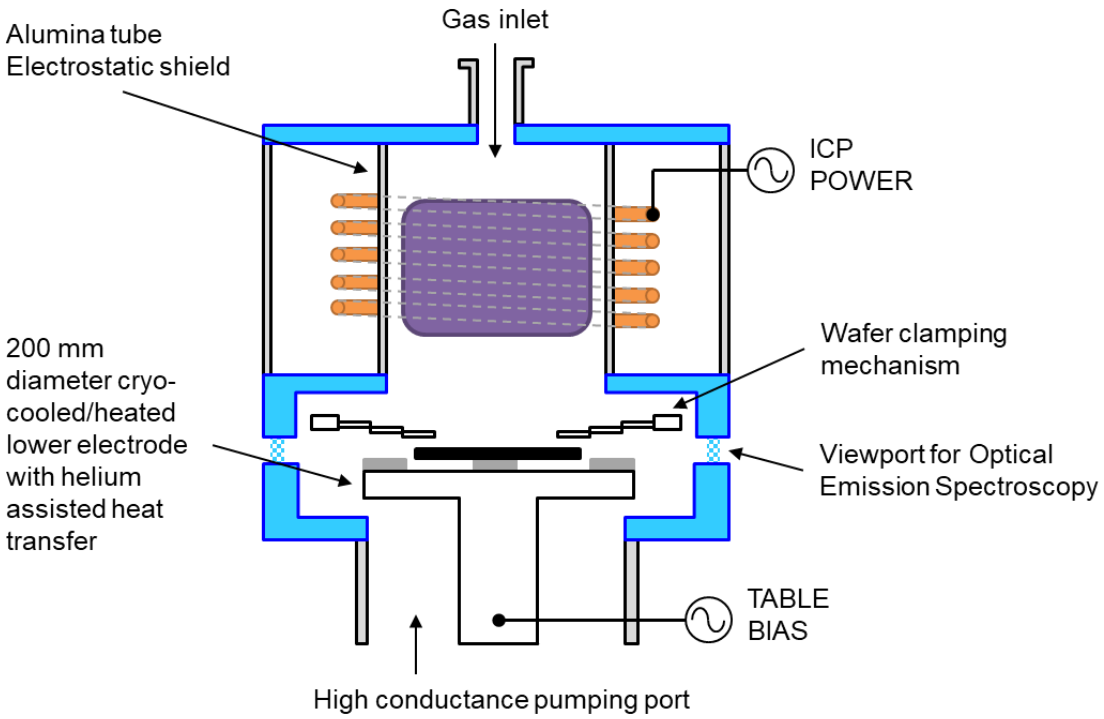

Figure 4.1 Schematic of the *Plasmalab System100* inductively coupled plasma system used.

ICP-RIE configuration has come to dominate high aspect ratio etching of silicon oxide. Such systems are simple, relatively cheap, and provide good process stability allowing straightforward process optimization.

Plasma processes in this work are performed in the Nanofabrication facility at the Molecular Foundry of Lawrence Berkeley National Laboratories. The system used for these processes is the Oxford Instruments Plasma Technology Plasmalab System 100 ICP etcher, schematically shown in Figure 4.1.

RF power (13.56MHz) is applied to both the ICP source (up to 3000 Watts) and substrate electrode (up to 600 Watts) to generate the etch plasma. An electrostatic shield around the ICP tube is used to ensure that the ICP power is purely inductively coupled, hence eliminating sputtering of tube material and minimizing unnecessary high energy ion damage to devices. Ion energy at the substrate is monitored by measurement of the DC bias generated on the lower electrode, and is controlled mainly by the RF power supplied to this electrode.

Wafers are loaded into the chamber via a load-lock to maintain good stability of chamber vacuum and hence repeatability of etching results. The wafers being etched are either mechanically clamped to the temperature-controlled lower electrode. Pressurized helium gas is applied to the back of the wafers to provide good thermal conductance between the chuck and the wafer. Where necessary, smaller samples are attached on 4" Silicon carrier wafers with thermally conductive glue.

The Plasmalab System100 ICP has control of substrate temperature to an accuracy of ±1 ˚C over a temperature range of –150˚C to +400˚C, through the use of electric heater elements and a supply of liquid nitrogen coolant circulating circuit. Substrate temperature has a marked effect on the etch result, as it controls the volatility of the etch species and hence influences the chemical component of the process, affecting not only etch rate, selectivity, and profile, but also surface roughness. The system can be operated over a pressure range from 1mT to 100mT allowing accurate control process chamber pressure.

Etching processes involve different mechanisms. In most cases, no reaction takes place between the neutrals and the material to be etched, despite the fact that a volatile product can form and the reaction between the atomic etchants (e.g., F and C atoms) and the substrate (e.g., SiO_2) is exothermic to produce the gaseous product (SiF_4 and CO_2). In this case, energetic ion bombardment speeds up the rate of reactions that generate gaseous products and anisotropic etching occurs. More details of SiO_2 etching using fluorocarbon base plasma are explained hereafter.

4.3 Plasma etching of Silicon oxide

F atoms react slowly with SiO_2 in the absence of ion bombardment (1/40th the rate of F + Si at room temperature).[181] This rate is too slow to cause much undercutting in most SiO_2 etching processes. Ion bombardment greatly accelerates the etching of SiO_2 by pure F atoms,[182] but because Si also etches rapidly under these conditions, this approach is not commonly used for silicon microelectronics applications. Instead, fluorocarbon plasmas are used for selective etching of SiO_2 over Si. Although the bulk of dielectric etching in IC fabrication is of lower dielectric constant insulators, etching of SiO_2 is still important.

Fluorocarbon plasmas etch SiO_2 in reactions that can form stable products SiF_4, CO, CO_2, and perhaps COF_2, or even $SiOF_2$. CF_2 and CF_3 radicals, generated by electron impact

dissociation and detachment of the feed gas, do not spontaneously etch SiO_2 in the absence of ion bombardment.[182] Neutral CF_x radicals and ions bombard surfaces and lead to the formation of a fluorocarbon film. The deposition of this thin film on horizontal surfaces is the most important aspect of the etching of SiO_2 in fluorocarbon-containing plasmas. Indeed, a thicker film is formed on Si than on SiO_2. The high selectivity of etching SiO_2 over Si was attributed to this difference in film thickness.[183, 184]

Unlike processes that rely on a sidewall film to suppress etching, the fluorocarbon film supplies reactants that are activated by ion bombardment. The film also improves selectivity toward etching of Si. The composition of the film and its deposition rate on SiO_2 depend on which fluorocarbon feed gas is used, the addition of other gases, the reactor materials, and other processing conditions. If the deposition rate is too fast, then the film continues to thicken and no etching occurs. Under useful conditions, a constant steady-state film thickness and composition are maintained while the underlying SiO_2 layer is etched at a constant rate.

4.3.1 Fluorocarbon plasma etching mechanisms of SiO_2

The etching mechanism for SiO_2 in fluorocarbon plasmas has been extensively studied in literature. Oehrlein and co-workers have extensively studied etching mechanisms for SiO_2 in fluorocarbon plasmas.[185-187] They found that the deposition rate of the fluorocarbon film depends on gas composition and DC bias voltage (Figure 4.2(a)). Lower ion energies favored faster deposition rates, displayed as negative values in Figure 4.2(a). If a fluorocarbon film was deposited at low ion energy and then, under the same plasma conditions, subjected to high ion energies was seen to etch. These net etching rates are given by the positive values in Figure 4.2(a). Under conditions when the etching rate for the fluorocarbon film is much slower than the deposition rate, a thick film continuously grows and no etching of the underlying SiO_2 occurs. If conditions are such that the film etching rate is much greater than the deposition rate, then little if any film will form on SiO_2. When the film etching and deposition rates are nearly equal, then the nature of the underlying material determines the steady-state film thickness. If it etches fast, as it does for SiO_2, then the film is relatively thin, while if it etches slower, as for Si, then a thicker film is present.

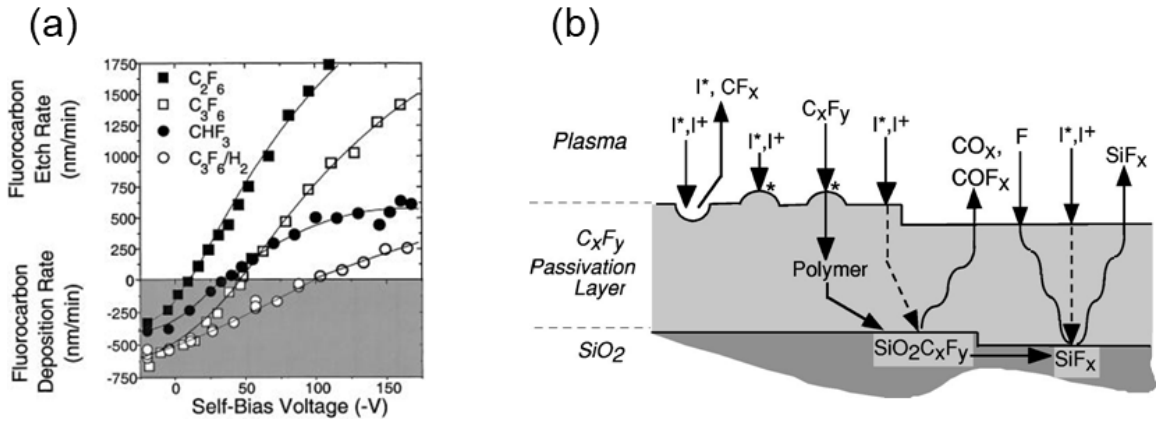

Figure 4.2 (a) Fluorocarbon etch rates as a function of self-bias voltage for different feed gases. The fluorocarbon substrate was deposited at 0 W RF bias power at the same process condition where the etch rates were determined. (b) Schematic of surface reaction mechanism for fluorocarbon etching of SiO_2. I^+ refers to an ion. I^* refers to hot neutrals. The dashed lines represent energy transfer through the polymer film. The curved lines represent species diffusion through the polymer.[187, 188]

Some of the processes that occur during etching of SiO_2 in fluorocarbon-containing plasmas are summarized in the schematic mechanism reproduced in Figure 4.2(b).[188] The film affects etching in two ways. First, it attenuates the energy of impacting ions that penetrate the film and reach the underlying layer. Ion-assisted etching rates typically decrease with the square root of ion energy above a threshold energy, hence, the thicker the film, the slower the etching rate.

This inverse dependence of etching rate as a function of film thickness is illustrated by Schaepkens and Oehrlein.[187] Somewhat surprisingly, SiO_2, Si, and Si-nitride all fall on the same curve. More recently, it was shown that the etching rate of Si, SiO_2, and Si-nitride scales inversely with the amount of fluorine in the film.[185] The explanation for this is that this fluorine is liberated by ion bombardment. Some of it diffuses to the underlying surface and participates in etching. Fluorine-containing products are liberated from the film; hence, fluorine content in the fluorocarbon film is reduced.

4.3.2 Phenomena in Silicon oxide dry etching

Charging in high aspect ratio features is believed to be responsible for "etch stop" that is often observed for dielectric materials.[189-194] Etch stop can also be caused by *deposition of fluorocarbon* polymer at the bottoms of high aspect features in insulating films.[195] The combination of charging and polymer deposition can cause other interesting

phenomena. When high aspect ratio holes are etched into an insulating film, a *twisting* is sometimes observed. It appears to be random; the origin is believed to be due to statistical variation in the amount of polymer and the amount of charge deposited on one side, causing the ions to be deflected off normal incidence, producing asymmetric profiles. Wang and Kushner simulated this twisting effect during etching of SiO_2.[196] The different panels represent different random seeds in the Monte-Carlo simulations. They find that once twisting begins in a feature, it propagates. This has to do with the fact that ions are neutralized on *glancing* collisions with the sidewalls. These neutrals then perpetuate the twisted trench or hole.

4.4 Future of SiO_2 Plasma etching

Better control of ion and neutral fluxes, as well as ion energy, will be required to address issues such as CD control, ARDE, line-edge roughness, and lattice damage due to ion bombardment. In addition, improvements in the precise control of amount of material removed and etch uniformity will be needed.

Bias power pulsing seems to offer an additional means for controlling ARDE, without changing pressure or gas flows, by operating in an ion limited regime.[197, 198] In this case, the neutral flux stays nearly constant, but ion-flux is controlled by the on/off cycle of the bias. Although etching rates may still be decreased by the increased aspect-ratio, the required longer etch times are not prohibitive. With bias pulsing, photoresist erosion is reduced more than the dielectric etching rates, increasing selectivity to photoresist as compared to continuous-wave plasmas.

Pulsed plasmas also allow very narrow ion energy distributions to be obtained for most of the afterglow period.[199, 200] By applying bias synchronously in the afterglow, a nearly monoenergetic ion energy distribution (IED) can be obtained. It should be noted that pulsed plasmas produce little Vacuum Ultra-Violet (VUV) light in the off portion, and therefore less average VUV light while maintaining high positive ion density. The ion flux during the off portion is reduced, so there should be a net gain in the ion-to-VUV photon flux ratio for pulsed plasmas, perhaps suppressing photo-assisted etching, photoresist degradation, and defect generation in sensitive regions of circuits.[201]

Atomic Layer Etching (or ALE) is an advanced etch technique that allows for excellent depth control on shallow features. As device feature size is reduced further and further ALE is required to achieve the accuracy required for peak performance.[16] The basic concepts of this technique are well address in the Introduction of this work (Chapter 1.).

High fidelity pattern transfer (etching) is essential for the fabrication of today's advanced microelectronic devices. As features shrink to sub-10nm levels, there is an increasing need for atomic-scale fidelity. This has led to a growing interest in ALE, which overcomes the limitations of conventional (continuous) etching at the atomic scale. Plasma-based atomic layer etching is a cyclical etching process of gas dosing and ion bombardment that removes material layer by layer and has the potential to remove single atomic layers with very low damage.[202]

4.5 Fluorocarbon-based ALE

Etching of silicon dioxide is an important part of integrated circuit manufacturing and has been a focus of ALE studies. For ALE of SiO_2, a fluorocarbon deposition approach was developed (Section 1.3.2) that provides both fluorine and carbon reactants in the modification step. For atomic layer etching of SiO_2 using fluorocarbon ions or precursors, computational work has been performed by Rauf[53] et al. and Agarwal and Kushner.[5] The molecular dynamics simulation of Rauf et al.[203] first showed the potential of a two-step etch process consisting of the formation of a nanometer-thick,[53] self-limited fluorocarbon passivation layer on a SiO_2 or Si surface followed by etching with Ar^+ ions with energies up to 50 eV using the deposited fluorocarbon as a source of etchant.[62] A sequence of these steps enabled nanometer precise etching of SiO_2 and Si.

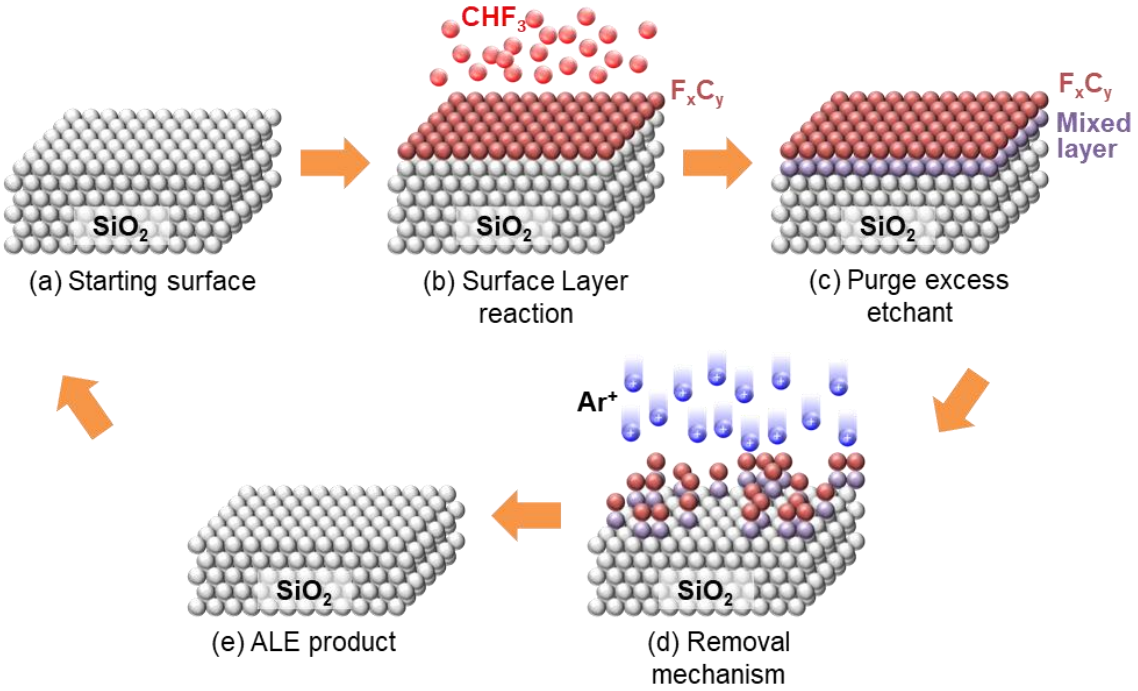

Figure 4.3 Concept of the SiO_2 atomic layer etching process, ALE etches monolayer by monolayer in a cyclic, self-limiting process. (a) SiO_2 starting surface (b) SiO_2 top monolayer is passivated in non-etching CHF_3 plasma. A fluorocarbon (FC) thin film is formed. (c) Reactive ions and neutrals are purged away from the chamber. FC passivation layer makes the top layer (the so-called mixed layer). Mixed layer can be more easily etched compared to sub-layers. (d) Remove the mixed layer using Argon ions from biased plasma (self-limiting). Ar ions are below the threshold energy for etching SiO_2 substrate. (d) Reactive product purged and self-limiting etching at 1 to several ML/cycle

Successful implementation of SiO_2 etching using Fluorocarbon atomic layer etching is shown in Figure 4.3.[52, 204] ALE of SiO_2 was investigated using the ICP reactor schematically shown in Figure 4.1. The substrate is powered at 13.56 MHz through a blocking capacitor. The wafer, 4 inches in diameter, sits in electrical contact with the powered substrate and is surrounded by dielectric focus rings. ICP allows for the investigation of the layer-by-layer etching of SiO_2 using low energy fluorocarbon and Ar^+ ions. ICP generates high density plasma and can be used to generate the following sequence of processes:

(i) the deposition of a thin fluorocarbon layer on the material surface using low energy C_xF_y ions;

(ii) the removal of the top layer of the material using Ar^+ ions in a manner that only the amount of material commensurate with F on the surface is removed through reactive ion etching.

The ALE process starts with the generation of steady-state Ar plasma during step (a) in Figure 4.3. Steady-state plasma is a plasma generated using only the ICP power. The steady-state plasma is not biased with the table electrode and results in a cloud of ions and radicals that are not accelerated toward the substrate. Steady-state plasma is maintained as long as the ICP power is upheld at a sufficient intensity (300 W) and the Ar gas flow is preserved (100 sccm).

The ALE process continues with the surface modification step (Figure 4.3(b)). Here, a pulse of 10 sccm CHF_3 is injected in steady-state Ar plasma for 3 seconds. Ar/CHF_3=91/9 gas mixture with a flow rate of 110 sccm was used. The CHF_3 is readily dissociated by electron impact, forming polymerizing radicals that create a fluorocarbon polymer film.[53, 62, 205] The goal is to rapidly deposit a single layer of fluorocarbon passivation which is sufficient to remove a monolayer (ML) of SiO_2. Since no table power was applied to the plasma, radicals do not have any directionality and will create polymer all round the ICP chamber. This step is followed by a purge step (Figure 4.3(c)). During this step with only the steady-state Ar plasma, the chamber is evacuated of any fluorine and carbon radicals. In addition, FC polymer reacts with SiO_2 creating a mixed layer as well described in Section 4.3.1. The polymer aids in the chemical sputtering of SiO_2 as the carbon in the polymer promotes removal of the oxygen in the SiO_2 while the F from the polymer aids in removal of the Si. The mixed fluorine SiO_2 layer on the surface can be etched with lower activation energy as compared to the underlying SiO_2 without modification.[206]

The etch process and polymer removal are initiated by high energy Ar ion bombardment. When the bias potential is applied at the steady-state Ar plasma the ion energy is increased to the above values and the FC film is rapidly etched, followed by SiO_2 etching. Once the FC is depleted the etch rates cease before the next precursor injection starts another cycle. Figure 4.3(d) and Figure 4.3(c) display the corresponding information for SiO_2. Ar ion energy has to be within the ALE windows of SiO_2, i.e. above the chemically enhanced etching energy threshold of FC polymer and mixed layer and below the physical sputtering energy threshold of SiO_2 (see Section 1.3.2).[184, 207]

Atomic layer etching is expected to have greater potential than conventional plasma etching to utilize the chemical nature of precursors and thus gain a new level of control over surface reactions. This ability is strongly reduced in continuous plasma processing, and has limited our possibilities of controlling surface reactions by choice of

precursor molecular structure. Either exposure of a substrate to precursor gases without plasma or short plasma exposures offer the prospect of retaining a much larger proportion of the precursor molecular structure at the surface, and in this fashion impact etching reactions. The exposure parameters can be varied over a significant range, with steady-state behavior as a limit.

Chapter 5 and 6 aim to demonstrate an atomic layer etching for patterning of silicon oxide with a cyclical fluorocarbon/argon plasma in a conventional inductively coupled plasma tool. To achieve a self-limiting behavior of the etching, the impact of plasma parameters and electrode temperature on the etch performance has been established. Atomic layer etching of silicon oxide with Ar and CHF_3 plasmas was previously addressed in literature[204] but this is the first account to the self-limiting behaviors in a conventional inductively coupled plasma tool. Ion bombardment energy during the removal step is tailored via the forward bias plasma power (RF power) to control the etching depth per cycle (EPC), reaching a self-limiting behavior. In addition, the impact of the electrode temperature on the etch performance is established. SiO_2 features can be patterned aspect-ratio independently using a self-limiting process ALE at -10 ˚C and low forward bias power (Chapter 6). Features with high aspect ratio etch with the same etching rate per cycles of those with low aspect ratios regardless of feature widths. The process studied here establishes the potential of the fluorocarbon atomic layer etching process for manufacturing features with low aspect ratio dependence.

Chapter 5

Atomic Layer Etching of SiO_2 with Ar and CHF_3 Plasmas: a Self-Limiting Process for Aspect Ratio Independent Etching

Overview

With ever increasing demands on device patterning to achieve smaller critical dimensions, the need for precise, controllable atomic layer etching is steadily increasing. In this Chapter, a cyclical fluorocarbon/argon plasma is successfully used for patterning silicon oxide by atomic layer etching in a conventional inductively coupled plasma tool. The impact of plasma parameters and substrate electrode temperature on the etch performance is established. Modulating the substrate temperature, it is possible to achieve self-limiting behavior of the etch process. At an electrode temperature of -10 ˚C, etching stops after complete removal of the modified surface layer as the residual fluorine from the reactor chamber is minimized. Lastly, this chapter shows the ability to achieve independent etching, which establishes the potential of the developed cyclic atomic layer etching process for small scale device patterning.

5.1 Fluorocarbon-based ALE of SiO_2 using cyclic Ar/CHF_3 plasma

Advanced nanomanufacturing is increasingly demanding atomic-scale process controllability to produce features with sub-10nm critical dimensions[14, 208]. The performance of the resultant devices depends critically on the etching step, presenting etch challenges that continue to increase as process requirements grow more stringent[1, 3]. The necessary control of surface properties in combination with the decrease in overall film thicknesses requires material selectivity and atomic scale control of etching directionality at the truly atomic scale[209]. Atomic Layer Etching (ALE) offers this level of control of etch performance, and has significant potential to overcome the challenges confronting modern nanofabrication techniques. The ALE process consists of two sequential steps: first, the surface of the material is chemically modified creating a thin reactive surface layer with well-defined, angstrom-scale thickness (Figure 5.1(a)). Second, in the etch step, the modified surface layer is selectively removed by bombardment with Ar ions (Figure 5.1(b)). The ions used during the etch step induce a chemical reaction between the absorbed species and the substrate. Importantly, physical ion bombardment allows for the directional etching required to generate high aspect ratio nanoscale features.

The separation of the chemical modification and subsequent etch steps enable the fluxes of neutral and charged particles to be independently optimized, despite their different transport methods.[16] By providing the ability to control the parameters of both charged and neutral particles independently, this process increases the accessible parameters space to include, for example, species fluxes and their relative ratios. The greatest benefit from ALE is achieved when both reactions, the chemical modification step and the etch step, are fully self-limiting. The use of self-limiting reactions allows for tolerance to over-exposure, which improves uniformity on length scales spanning orders of magnitude.

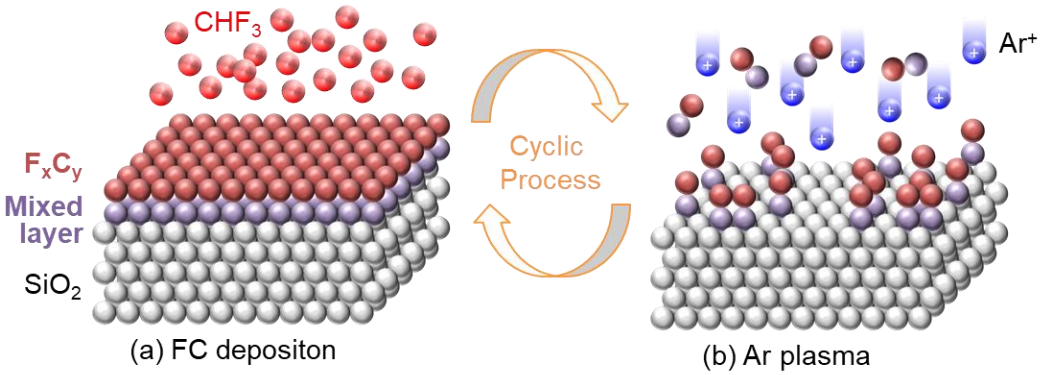

Figure 5.1 SiO_2 atomic layer etching process with Ar and CHF_3 Plasmas. (a) Deposition of a thin fluorocarbon layer on the material surface using low energy C_xF_y ions. A fluorinated SiO_2 layer (mixed layer) is created. (b) Removal of the top layer of the material using Ar^+ ions in a manner that only the amount of material commensurate with F on the surface is removed through reactive ion etching.

The reported ALE process also allows to reach aspect ratio independent etching (ARIE), which refers to the independence of vertical etch rate on the aspect ratio of the features being etched.[155, 210] Additionally, by taking advantage of the surface selectivity of the plasma chemistry, ALE also offers reduced surface damage and an uncommon substrate specificity.[5, 209] Over the past decade, ALE has been realized for a variety of materials including but not limited to Si, SiO_2, Si_3N_4, Al_2O_3, and HfO_2.[16, 51, 62, 204, 211, 212]

SiO_2 is one of the most important materials in semiconductor nanofabrication.[213] The mechanism behind continuous etching of SiO_2 has been widely studied.[1, 187] Selective etching of SiO_2 over Si and Si_3N_4 can be performed in inductively coupled plasma (ICP) using fluorocarbon plasmas, and the etch rate is inversely proportional to the thickness of the fluorocarbon (FC) film deposited on the surface.[214, 215] Computational investigation of plasma assisted ALE of SiO_2 showed that when the plasma chemistry and plasma ion energies during each step are controlled, it is possible to reach a self-limiting etching process.[5] ALE of SiO_2 was then evaluated using cycles of inductively coupled Ar and fluorocarbon plasmas.[52]

ALE of SiO_2 with fluorocarbon plasmas is realized by passivating the surface with an angstrom-thin fluorocarbon layer followed by Ar ion etching. The fluorocarbon layer lowers the binding energy of the SiO_2 surface atoms with the underlying lattice, creating an energy window where incoming Ar ions can sputter the modified surface layer, but do not have enough energy to remove pristine SiO_2 sites.[176, 185] Here, we develop a self-limiting ALE

process of SiO_2 using fluoroform (CHF_3). To avoid the use of specialized equipment, which is also undesirable from a cost perspective, we have optimized the process for use in a conventional ICP tool.[216] We first investigated the etch step using low energy Ar ion bombardment (section 5.3.2). In a plasma environment, the ion energy distribution controls the physical sputtering and the extent of damage to the substrate. By carefully tailoring the ion bombardment energy via the forward bias plasma power (RF power), we demonstrate control of the etching depth per cycle (EPC), reaching a self-limiting behavior. We also found that the substrate temperature critically controls this self-limiting behavior (section 5.3.3). We showed that the amount of fluorocarbon polymer formed on the SiO_2 increases as the substrate temperature is reduced, ultimately controlling the etch step. The gradual change in the self-limiting EPC is due to the residual fluorine radicals in the ICP chamber that are released during the Ar bombardment. Ultimately, we show that self-limiting and aspect-ratio independent ALE is achieved combining a substrate temperature of -10 ˚C and low forward bias power (section 5.3.4).

5.2 ALE using conventional plasma processing tool

5.2.1 Experimental apparatus and plasma analysis

All work was performed using a Plasmalab System 100 ICP etcher from Oxford Instruments Plasma Technology. In a typical process, the wafers are loaded into the chamber via a load-lock and mechanically clamped to a temperature-controlled substrate holder. The substrate electrode was cooled with liquid nitrogen, allowing precise control of the substrate temperature from -150 ˚C to 400 ˚C. The chamber wall temperature was fixed at 60 ˚C. Radio frequency (RF) power (13.56 MHz) was applied to the ICP source (up to 3000 W) and the substrate electrode (up to 500 W) to generate the plasma. The RF power supplied by the substrate electrode generates a DC bias that controls the ion energy at the substrate.

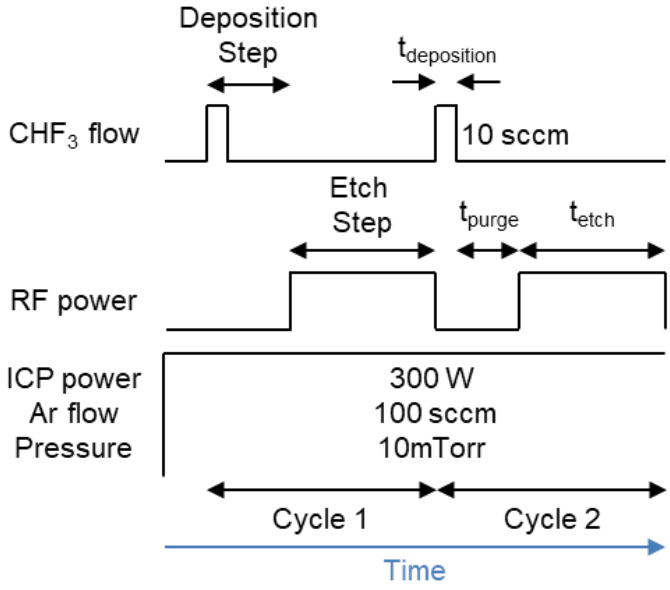

Figure 5.2 Schematic of fluorocarbon-based ALE. The ALE experiment was conducted with a continuous, steady-state Ar plasma and repeated ALE cycles. Each cycle consists of a fluorocarbon polymer deposition step and a low energy ion bombardment etch step. The deposition step is unbiased (RF power off), and starts with a short CHF_3 injection followed by a chamber purge. The etch step is biased (RF power on), and its duration (etch time) was varied to optimize self-limiting behavior.

Plasma parameters, including ion energy distribution (IED) and total ion flux were measured using a commercial retarding field energy analyzer (RFEA) Semion™ System 500. The sensor was mounted on a 4-inch Si wafer, with the front face parallel to the lower electrode surface, perpendicular to the direction of ion travel. The analyzer was biased with a potential sweep to discriminate Ar ions with different energies. The IED was determined from the ion-current characteristic, while the ion flux was determined by integrating the measured IED. The complete description of the analyzer is reported elsewhere.[217, 218]

5.2.2 Fluorocarbon ALE

We used Si substrates with 100nm of thermally grown SiO_2 to develop the ALE process. The SiO_2 test samples (0.5 x 1 in^2) were positioned on 4-inch Si carrier wafers and kept in place using Fomblin oil, which granted mechanical stability and improved the thermal contact and between sample and carrier. To establish consistent process parameters, the samples were loaded after a chamber cleaning and conditioning procedure comprised of an oxygen plasma cleaning followed by an Ar plasma preconditioning and 30 cycles of the main ALE process. We used spectroscopic ellipsometry (UVISEL, Horiba) to

quantify the extent of material modification and etch depth. For unpatterned SiO_2 on Si substrates, the ellipsometry data were fitted using a two-layer optical model, which consists of a fixed bottom Si layer and a varying top layer. The top layer represents a combination of SiO_2, fluorinated SiO_2 (mixed layer), and fluorocarbon. This optical model provides a good approximation of the data since the optical properties of the FC layer, the mixed layer, and the SiO_2 layer are similar.[184] The small differences in refractive indices of the FC and mixed layers are dwarfed by the large differences in thickness between the fluorocarbon (angstroms) and the SiO_2 layer (100nm). SE measurements are subject to random and systematic errors. Unfortunately, systematic errors can be the most important errors in some experiments, and therefore must be estimated and incorporated into the data analysis in some way. Of course, after the random and systematic error limits of the data have been estimated, it is necessary to propagate these errors into the actual data being fit.[78] For this reason the SE data in section 5.3.2, 5.3.3 have a systematic error of ± 0.8 Å/cycle.

Figure 5.2 shows a schematic ALE process sequence. During the entire process, there was continuous Ar flow at 100sccm. The chamber pressure was held at 10mTorr, and the ICP power held constant at 300W. For the deposition half-cycles, short periodical injections of 10 sccm of CHF_3 were introduced. The injection time ($t_{deposition}$) was varied to achieve the desired deposition thickness of 5Å. We found that for $t_{deposition}$ = 3s the mass flow controllers (MFC) produce a stable and reproducible fluorocarbon injection. After the CHF_3 pulse, a purging step (t_{purge} = 30s) with pure Ar plasma ensures that all the fluorocarbon compounds are exhausted from the process chamber. The deposition and purge steps were unbiased (0 V DC bias). During the etch half-cycle, RF power was applied to generate a DC bias in the range of 0-50V. Powered electrodes caused the Ar ions to be accelerated toward the SiO_2 with low ion energy. Different etch step lengths (etch time or t_{etch}) were also explored.

5.3 ALE Self-limiting behavior

5.3.1 Plasma Diagnostic for ALE

Self-limiting surface reactions are required to control the etch depth per cycle independently of etching time. To achieve true ALE etching, both spontaneous chemical etching during the deposition step and physical sputtering of unmodified SiO_2 during the

etch step should be minimized. In the deposition step, the CHF_3 pulse is followed by a purging step where any CHF_3 residual is evacuated from the chamber. After the deposition step, the fluorocarbon layer reacts with the substrate surface below, lowering the threshold energy necessary to remove material from the surface compared to pristine SiO_2. The nature of the interaction of Ar ions with surface species is in part determined by the ion energy. Ar ions gain energy when they are accelerated through the plasma sheath, which in turn means that the Ar ions energy is proportional to the RF forward power. When the process parameters are adjusted such that the Ar ion energy is above the threshold for ion activated chemical sputtering of the FC-mixed layer, but still below the threshold for SiO_2 physical sputtering, it is possible to selectively remove the modified surface layer without damaging the underlying unmodified SiO_2. The ions from the plasma incident on the SiO_2 surface can have a broad energy distribution that dictates the physical sputtering rate and extent of substrate damage. To avoid this, careful adjustment of the Ar ion energy is instrumental in controlling the ALE process. Below, we demonstrate how the ion energy distribution of the ions impinging on the wafer can be adjusted by applying RF power to the substrate.

Figure 5.3(a) shows the measured ion energy distribution (IED) of the Ar plasma as a function of RF power applied to the lower electrode. The IED measuring techniques are critically important and are discussed in section 1.5.2 of the Introduction chapter. All experimental data presented were collected using pure Ar plasma with 300 W inductively coupled source power. The IED curves showed in this section were averaged over a series of five scans, in order to increase the signal to noise ratio. When the electrode is grounded (0 W RF power), the ions accelerated from the bulk plasma to the electrode acquire an energy equal to the floating sheath potential. The IED exhibits a single peak with average ion energy of 7 eV. With increasing RF power, the IED shifts to larger values. At RF power of 4 W, a second peak starts to evolve in the IED. As the RF power is further increased the bimodal peak separation increases. At RF power of 10 W, the IED consist of two clearly discernable peaks at about 40 eV and 55 eV. The IED of pure Ar plasma is a good approximation of the plasma used during the etch step, where the chamber has been evacuated for any residual fluorine.

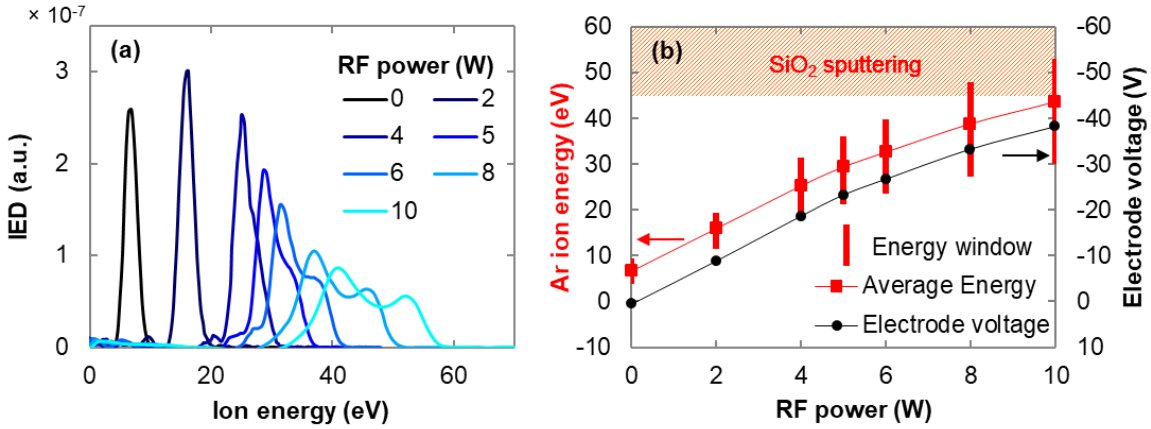

Figure 5.3 (a) Measured ion energy distribution (IED) for different values of the RF bias applied to the lower electrode. Experimental parameters are 10mTorr chamber pressure, 300 W ICP power, and 100 sccm Ar flow. (b) Measured electrode voltage (DC bias) and average energy of the measured IED function as a function of the discharge power. The error bars quantify the width of the distribution. They denote the energy window comprising 98% of the integrated area of the IED.

This shape evolution of the IED will be crucial in the ALE processes. Even though the average ion energy (Figure 5.3(b)) may be lower than the threshold for sputtering bare SiO_2 (45 eV),[62] the maximum energy of the IED can exceed this energy threshold. The average energy of the measured distribution function and the time averaged electrode voltage (often referred as electrode voltage or DC bias) are determined using the retarding field energy analyzer. These parameters are plotted in Figure 2(b) as a function of the RF forward power. The indicated error bars denote the energy distribution which comprises 98% of the area under the IED curve. In other words, 1% of the Ar ions in the plasma has an energy smaller than the lower error bars and 1% has an energy higher than the upper error bars. From this representation, we can conclude that the Ar plasmas with RF powers higher than 8 W (DC bias larger than -33 V) have significant contributions of ions with energies above the threshold for sputtering SiO_2 and must be avoided.

5.3.2 DC bias optimization

The need for fine control of RF power is illustrated by Figure 5.4(a), showing the SiO_2 removal when the Ar plasma was biased at different RF powers, both with ($t_{deposition}$ = 3 s) and without ($t_{deposition}$ = 0 s) fluorocarbon deposition step. The process without the fluorocarbon deposition step corresponds simply to the sputtering rate of SiO_2 for different values of the DC bias. We find that at a DC bias below -19 V, no SiO_2 removal occurs. As the DC bias is increased above -19V, we observe sputtering of SiO_2. In particular, we observed a

significant acceleration of this physical etching for DC bias higher than -33 V. At this voltage the IEDs exceed the SiO_2 sputtering window. However, even for DC bias of -23 V and -27 V, where the IED is nominally below the sputtering threshold of SiO_2, we detected a measurable sputtering rate. We understand this sputtering to be caused by very low concentrations of impurities in the substrate as the sputtering threshold is very sensitive to SiO_2 chemistry.[62] In turn, it is necessary to keep the DC bias below -19 V to avoid any ambient SiO_2 sputtering.

The introduction of a fluorocarbon surface modification is introduced via a 3 s CHF_3 gas pulse. This adsorbs the chemical reactant to SiO_2 (Figure 3(a), $t_{deposition}$ = 3 s), and allows the material to be etched with lower activation energy compared to the unmodified SiO_2 (45 eV).[62]

One of the main advantages of ALE is the opportunity to separate the FC-SiO_2 chemical surface modification from the physical removal of the surface layer. Separation of reactions allows for the decoupling of the generation and transport of ions, electrons and radicals and facilitates self-limiting reactions.[219] Self-limiting reactions are reactions that slow down as a function of time (Figure 1.3). Here, etching takes place in an initial time followed by a removal rate that approaches zero. In Figure 5.4(b) we evaluated the amount of material etched per cycle when the etch step length is increased from 0 s to 180 s. At 0 s no SiO_2 etching is detected and a thin fluorocarbon film (3 Å thick) is deposited on the surface. The etch step is approaching a self-limiting regime when the DC power is reduced from -19 V to -9 V. The dashed curve in Figure 5.4 shows a hypothetical self-limiting behavior for the parameters reported here. For -9 V DC bias the EPC has the largest variation in the first 60 s, reaching 11 Å/cycle. A quasi-ALE behavior is observed, where the EPC does not completely saturate but slightly increases in the following 120 s. The need to reach complete saturation of SiO_2 EPC over etch time made us extend the study of SiO_2 ALE to different substrate temperatures.

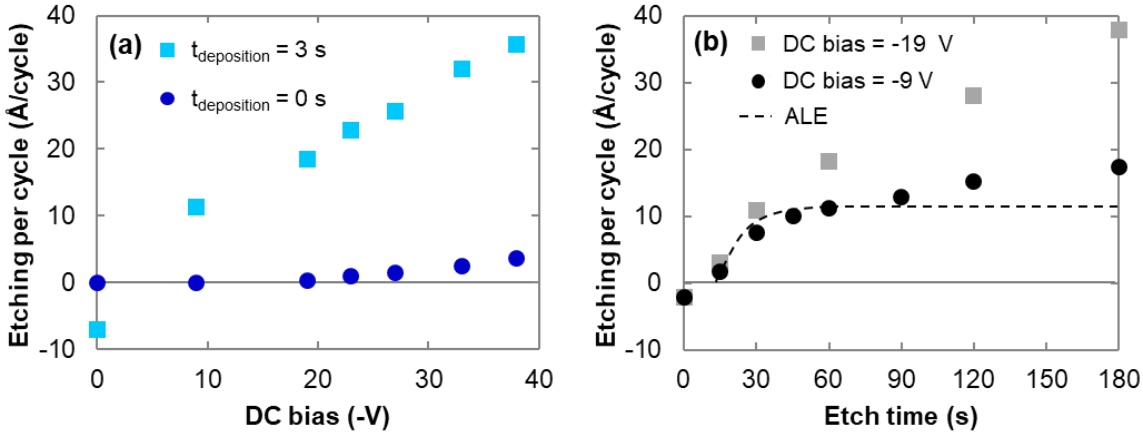

Figure 5.4 SiO_2 etching per cycle in a conventional PlasmaLab 100 ICP tool at 300 W ICP power, 10 mTorr pressure and 30 s purge. The substrate temperature is fixed at 20 ˚C. (a) SiO_2 etching per cycle vs DC bias, with ($t_{deposition}$ = 3 s) and without ($t_{deposition}$ = 0 s) the fluorocarbon dosing step. The etch time is fixed to 60 s. Without the chemical modification step no detectable etching of SiO_2 occurs for a DC bias smaller than 20 V. A systematic error of ± 0.8 Å/cycle associated with SE data is considered for each point in the pot. (b) SiO_2 etching per cycle vs etch time, for two DC bias values: 9 V and 19 V. Dose time is fixed to 3 s. A systematic error of ± 0.8 Å/cycle associated with SE data is considered for each point in the pot. In curve, "saturation curve" showing self-limiting removal in ALE.

5.3.3 Temperature control

The substrate temperature significantly impacts the sticking coefficient of the FC polymer deposited on SiO_2. The sticking coefficient is expected to increase with decreasing temperature.[220] The deposition step is essential to establish ALE. To allow high aspect ratio etching of features with small critical dimension, the sidewall FC layer needs to be thin and penetrate deep into the feature. The importance of the FC sticking coefficient on SiO_2 is reinforced by the increase of FC deposition with decreasing temperature. Figure 5.5**(a)** shows the SiO_2 etching rate per cycle as a function of etch step time and temperature between 20 ˚C and -40 ˚C. Temperatures as low as -60 ˚C were also explored, but no substantial benefits were detected. The data collected at t_{etch} = 0 s have negative values and correspond to the FC deposition rate on the SiO_2 surface. The values for the FC film thickness deposited per cycle as a function of temperature are plotted in Figure 5.5**(b)**. Moving from room temperature to -40 ˚C, the deposition per cycle changed approximately linearly from 2 Å/cycle to 7 Å/cycle. The change in the FC deposition rates strongly impacts the curves in Figure 5.5a).

Working in true ALE regime, the EPC vs etch time would show a self-limiting behavior, meaning that SiO_2 etching is happening in an initial "burst" but after consuming the FC film the etch stops and the EPC remains constant in value. For this reason, we defined a quantity that measures how much in percentage the curves in Figure 5.5(a) deviate from saturation after 60 s etching. This deviation from the self-limiting behavior was determined by calculating $\left[\frac{\text{EPC(180 s)-EPC(60 s)}}{\text{EPC(60 s)}}\right]$ (100 %), where $\mathbf{EPC(t_{etch})}$ is the etching per cycle of SiO_2 using an etch step of t_{etch} s. This quantity is calculated for each curve at different temperature and the results are plotted in Figure 5.5(c).

As evidenced in Figure 5.5(c), etching per cycle approaches a self-limiting behavior at a substrate temperature of -10 ˚C. At this temperature the EPC after 60 s is 9.5 Å/cycles and for the following 120 s it only changes 20 %, reaching a value of 11.5 Å/cycles. For temperatures different than -10 ˚C the curves in Figure 5.5(a) divert from self-limiting behaviors. From our data, we can conclude that the atomic layer etching of SiO_2 is subject to two different contributions that are minimized at -10 ˚C. For electrode temperatures higher than -10 ˚C, it is proposed that the etching rate increases because of residual fluorine in the chamber. Fluorine coming from the chamber walls and fluorocarbon polymer removed during the etch step are just two fruitful sources of residual fluorine in the ICP. Higher temperatures enhance SiO_2 chemical etching by fluorine.[221] This result was experimentally confirmed by first fluorinating the chamber walls with pure SF_6 plasma (50 sccm SF_6, 2000 W ICP, 0 V DC bias) and then running a pure Ar plasma (300 W ICP, -9 V DC bias). SiO_2 etching was evaluated during the pure Ar plasma. With clean chamber walls no SiO_2 etching was detected but when the chamber walls were fluorinated the Ar plasma etched the SiO_2 at a rate of was 9 Å/min, 0.5 Å/min, and 0 Å/min at substrate temperatures of 20 ˚C, -10 ˚C and -40 ˚C, respectively. This result proves the strong effect of substrate temperature on the chemical etching caused by residual fluorine radicals, but it also showed that for substrate temperatures lower than -10 ˚C the impact of fluorine contamination from the chamber walls on the etch process is negligible. In addition, continues etching of SiO_2 with fluorine shows an etch rate that increases strongly for increasing temperatures, suggesting an increase of reactivity between the FC film and the SiO_2 at high temperatures.[221, 222]

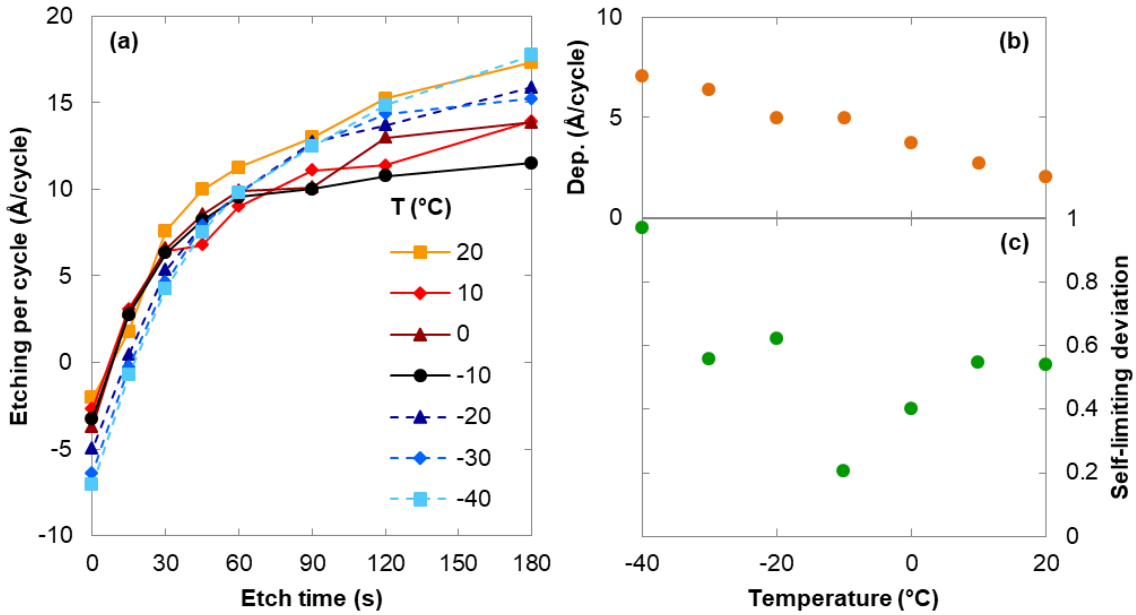

Figure 5.5 (a) SiO_2 thickness changes over Ar plasma etching time during one ALE cycle with varying substrate temperature, following fluorocarbon deposition of 3 s and purging the reactor chamber for 30 s. A systematic error of ± 0.8 Å/cycle associated with SE data should be considered for each point in the pot. (b) Measured thickness of the fluorocarbon film deposited on SiO_2 during one ALE cycle as a function of the substrate temperature. A systematic error of ± 0.8 Å/cycle associated with SE is be considered for each point in the pot. (c) Deviation of the etch per cycle from self-limiting behavior defined as **(EPC(180 s) – EPC(60 s))/ EPC(60 s)**. Self-limiting behavior of the etching is achieved for a substrate temperature of -10 °C.

The FC layer deposition plays an opposite role. We know that the etching of SiO_2 occurs during the Ar ion bombardment phase when SiO_2 is converted to fluorinated-SiO_2 by mixing with FC polymer.[223] Since the entire FC layer must be consumed during the etch step, the amount of SiO_2 etched is proportional to the initial polymer thickness. The reaction of the FC polymer with SiO_2 happens continuously during the Ar ion bombardment step with further FC-mixing reactions and hence SiO_2 removal happening throughout, until the polymer is fully depleted.[223] This results in an EPC that depends on polymer thickness, which in turn depends on electrode temperature. For high substrate temperatures, the FC layer deposited is thinner and the etching of SiO_2 terminates once all the polymer is consumed. For lower temperatures, a thicker polymer is deposited during each cycle, and a longer etch time is needed to completely remove the fluorinated-SiO_2. This implies that the EPC curves at substrate temperatures below -10 °C may still reach saturation but at a higher EPC and at a longer etch time.

We have demonstrated that ALE of SiO_2 is possible via the present method. ALE at -10 ˚C is the best process identified for pattern transfer, as described in the following section. However, the window for ALE is significantly restricted due to limitations at either end of the process window. First, it is clear that there is a consistent level of fluorine in the chamber at all times, likely due to desorption from the chamber walls as well as release from the FC polymer during etching. At temperatures above -10 ˚C the fluorine chemistry combined with the Ar plasma results in direct, uncontrolled SiO_2 etching. At mildly lower temperatures, however, the sticking coefficient of the FC is too high resulting in excess polymer deposition and increased interlayer formation. This also results in non-ALE behavior. Due to these two conflicting limitations, the ALE window is significantly limited. Further development of tool and process design is ongoing to allow for an increased ALE window by minimizing these effects.

5.3.4 SiO_2 patterning using FC-based ALE

Finally, hard mask definition was then carried out using our optimized process after metal lift-off. First, nanoscale features were created using electron-beam lithography on PMMA resist with trenches drawn from 20-200 nm with a mask thickness around 60nm. E-beam evaporation was then used to deposit 12nm of Cr at a pressure of 2×10^{-6} Torr. A final lift-off process used to define the Cr lines was performed with Remover PG (MicroChem) followed by acetone cleaning in an ultrasonic bath.

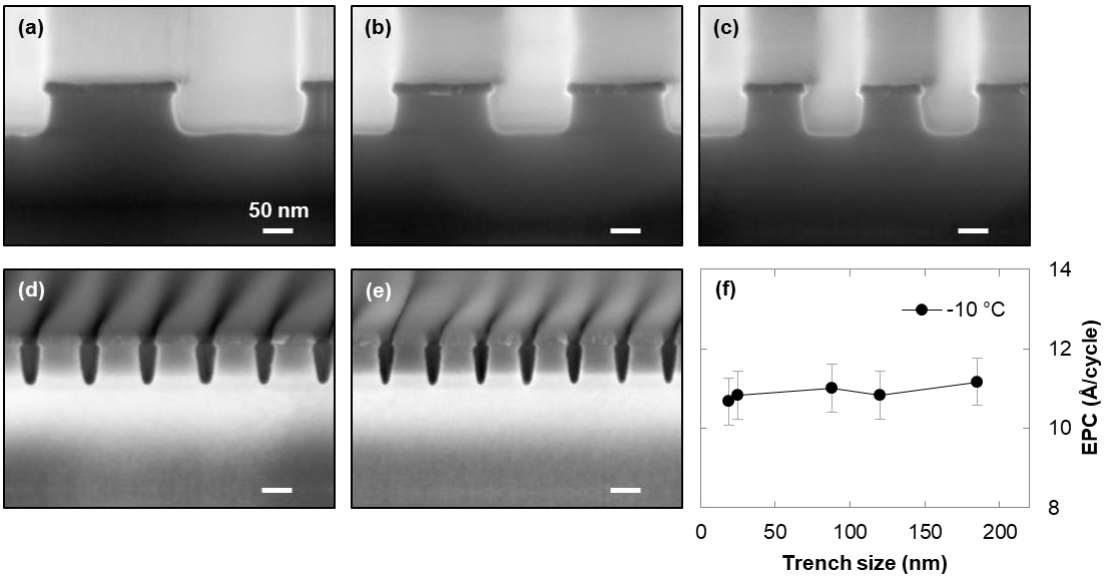

Figure 5.6 (a) – (e) Cross-sectional SEM images of silicon oxide features patterned using FC-Ar ALE. Experimental parameters are DC bias 9 V, ICP power 300 W, T = -10 ˚C. Different trench sizes after 60 ALE cycles: 200, 150, 100, 50, 40 nm from (a) to (e). (f) Etching per cycle from nano-sized trenches with electrode temperature at -10 ˚C. Errors bars indicate the uncertainty from the SEM measurement. Within the errors bars, different feature sizes are all etched at 11 Å/cycles.

Figure 5.6(a)-(e) show the Cr features after being etched for 60 ALE cycles under optimal ALE self-limiting conditions for flat surfaces, *i.e.* DC bias = 9 V, ICP power = 300 W and T = -10 ˚C, t_{etch} = 60 s. All features present the same vertical profile and a slight undercut is observed. Our process achieved the goal of aspect ratio independent etching. Features with large aspect ratios etch as fast as those with low aspect ratio regardless of feature width. The slight undercut beneath the mask can be caused by chemical and/or kinetic processes: e.g., ions and radicals reflected from the edges of the feature, broad Ar ions angular distribution, or residual fluorine from the chamber wall.[224] Ions scattered from feature edges can perhaps be ruled out since the sidewall profile does not change significantly with feature width. Regardless of the precise cause, it is clear that in order to achieve features free of undercut and therefore true atomic layer etching, one needs to find a careful balance between the Ar ion parameters (energy and angular distribution) and the fluorocarbon chemical reactant.

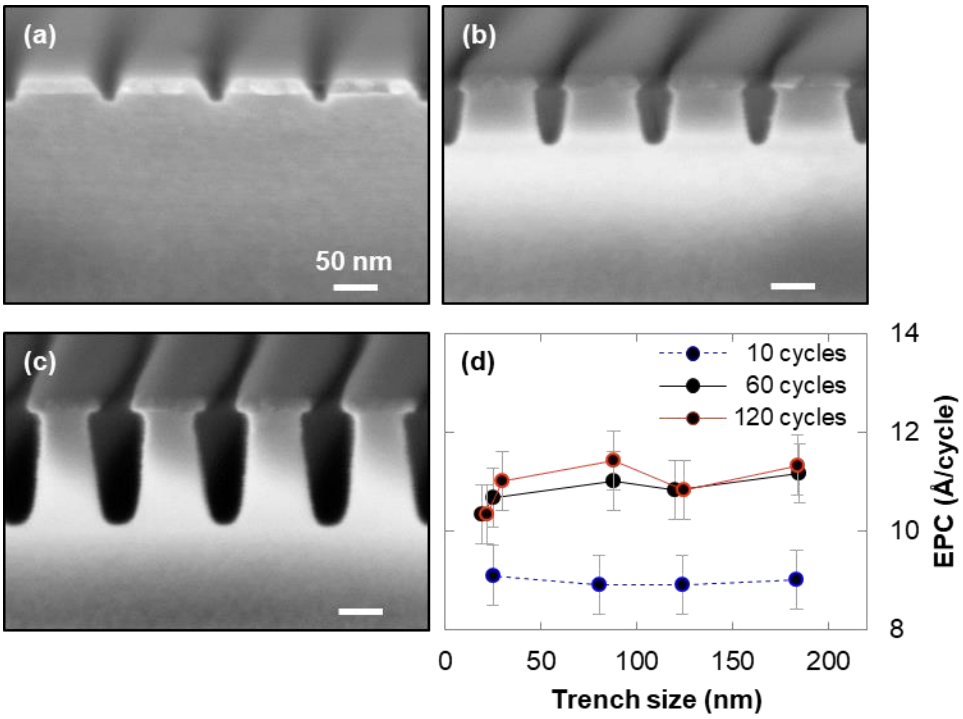

Figure 5.7 (a)-(c) Cross-sectional SEM images of SiO_2 features patterned using FC-Ar ALE. Experimental parameters are DC bias 9 V, ICP power 300 W, T = -10 °C. Each sample was etched for a varied number of ALE cycles: (a) 10 cycles, (b) 60 cycles and (c) 120 cycles. (d) Etching per cycle from nano-sized trenches under various numbers of cycles. As the trenches are etched deeper, the EPC increases.

We studied the evolution of SiO_2 trench profile over an increasing number of ALE cycles. Figure 5.7(a), (b) and (c) show 30nm features etched on SiO_2 for 10, 60 and 120 cycles respectively. After 10 ALE cycles, SiO_2 is etched and the etch depth is approximately 8.5nm. After 60 ALE cycles, SiO_2 has etched 64nm (corresponding to an average EPC of 10.7 Å/cycle). Further increasing the number of cycles causes the SiO_2 averaged EPC to remain constant. We clearly observed an increase in the EPC for 60 cycles compared to 10 cycles (Figure 5.7(d)). Other authors have similarly reported a gradual increase in the EPC as a function of the cycle number.[179, 223] It follows that a fluorocarbon film gradually builds up on the reactor walls during each ALE cycle. This fluorocarbon buildup over the course of the sequential ALE cycles provides an additional source of fluorine during the etch step, increasing the EPC.

Notably, the features investigated in Figure 5.7(c) are 5:1 aspect ratio SiO_2 over Cr trenches. The high selectivity of ALE enables the exposed SiO_2 features to maintain their

dimensions while being etched during 120 cycles. The pattern profile shows the successful patterning of silicon dioxide with high selectivity to Cr and the possibility to obtain high aspect ratio features.

5.4 Conclusion

In summary, we have shown that by using Ar plasma, periodic injections of CHF_3 and Ar ion bombardment in a conventional plasma tool, atomic layer etching of SiO_2 is possible. Low energy ion bombardment is crucial for minimizing the physical sputtering of SiO_2. This has been studied using a retarding field energy analyzer, and we demonstrated that the Ar ion energies are within the ALE window. A few angstroms of deposited fluorocarbon layer combined with low energy Ar ion bombardment is used to control the etching of SiO_2. Using ellipsometry, we studied the SiO_2 etch per cycle relative to the etch step time as a function of substrate temperature. At -10 ˚C the contributions to chemical etching coming from fluorine radicals and fluorocarbon compounds from the chamber walls are minimized and a quasi-self-limiting behavior ALE is observed after 60 s etch time. However, deviation from self-liming ALE behavior and undercut during SiO_2 pattern transfer clearly indicates the presence of a secondary supply of fluorine from the chamber walls. Additionally, during the initial stages of the etch, the fluorocarbon film buildup over multiple ALE cycles causes an increase in EPC with the number of ALE cycles. Future work will be focused on studying the chamber wall chemistry and finding solutions to mitigate its adverse effects. Overall, using ALE at -10 ˚C we reduced geometric loading effects during etching and reached aspect ratio independent ALE. This type of process enables high flexibility and tunability in terms of precursors, ion energies, fluorocarbon film deposition, substrate temperature, and etch time to further decrease critical dimensions towards the atomic scale pattering era.

Chapter 6

Balancing Ion Parameters and FC Chemical reactants for SiO_2 Pattern Transfer Control using Fluorocarbon-Based Atomic Layer Etching

Overview

This chapter presents a study of the evolution of etch profiles of nanopatterned silicon oxide using a chromium hard mask and a CHF_3/Ar atomic layer etching in a conventional inductively coupled plasma tool. Substrate electrode temperature, chamber pressure, and electrode forward power strongly affect the etch profile evolution of nanopatterned silicon oxide. Chamber pressure has an especially significant role. Indeed, lower pressure leads to lower etch rates and higher pattern fidelity. Notably, at higher electrode forward power, the physical component of etching increases and more anisotropic etching is achieved. By carefully tuning the process parameters, aspect ratio independent etching and high fidelity pattern transferring are achieved. Trench sizes ranging from 150 to 30 nm can be all etched with a sidewall angle of 87˚±1.5˚ and undercut values as low as 3.7±0.5%. Furthermore, this chapter provides some guidelines to understand the impact of plasma parameters on plasma ion distribution and thus on the atomic layer etching process.

6.1 Application of fluorocarbon-based ALE to device patterning

The demand for atomic-scale surface engineering and process controllability in advanced manufacturing and technologies has grown steadily in the latest years.[2] Critical dimensions and required pitch shrinkage call for increasingly higher etching precision and selectivity,[1, 3, 4, 133] with the additional need for developing new processes to accommodate the increasing complexity in device structures.[225] Atomic Layer Etching (ALE) offers unmatched levels of control for etching performances, as required by the new technology node, and holds a great deal of potential to confront and overcome the challenges in modern nanofabrication techniques.[208]

In plasma-enhanced ALE, an inert plasma is typically maintained throughout, while alternating cycles of a reaction chemistry step, with a pulsed injection of precursors, and an etch step, when increased ion energy is applied to the wafer.[52, 204] A fluorocarbon (FC) chemistry is used to deposit Angstrom-thick layers on SiO_2 to provide the reactant adsorption. A thin fluorinated SiO_2 surface layer (mixed layer) is then formed. Subsequently, low energy Ar ion bombardment is used to remove both the FC layer and the mixed layer. When Ar ions have energies below the threshold for SiO_2 physical sputtering, the etching is stopped right after the mixed layer has been removed,[53] ergo ALE is a self-limiting process.[62] To realize the FC layer deposition, we use pulsed CHF_3 injections into unbiased Ar plasma.[207] Keeping the substrate unbiased is integral to achieve a precise FC film thickness control, in the range of one to few Å. Following FC deposition, a small forward bias plasma power (radio frequency [RF] power) is applied for 60 s. Powered electrodes cause the Ar ions to accelerate toward the SiO_2 with maximum ion energies below the energy threshold for physical sputtering of unmodified SiO_2. At the end of a cycle, the process sequence is repeated to achieve precise control over the total etched thickness.

Despite the benefits of atomic layer etching, few demonstrations in patterning of SiO_2 using CHF_3/Ar plasma have been reported. The main goal of Chapter 6 is the optimization of the SiO_2 etching profile for nanoscale-sized features (30-200 nm), which we tackle by investigating the effect of each plasma parameter on the whole ALE process. Such an in-depth study allows us to critically identify the extent of each parameter's impact and therefore to design the ideal process to obtain nanoscale-sized, aspect-ratio independent features. Moreover, the thorough understanding of the effect of such parameters as the substrate temperature, pressure, and forward bias power on the etched

profiles enables an indirect feedback loop that allows us to infer the plasma parameters by evaluating the resulting etched features.

In a previous study,[226] we reported the first demonstration of aspect ratio independent ALE and the achievement of the theoretically predicted self-limiting behavior, and therefore provided a guideline recipe for an optimized SiO_2 patterning at the nanoscale level (down to 30nm feature size). In addition, we showed the synergy of the ALE process: the combination of the FC deposition step and the Ar etch step causes SiO_2 etching. We developed our process in a conventional ICP tool, which provides the additional benefit of enabling a cost-effective process and straightforward transfer to scale production protocols in the manufacturing industry.

Here, we present the profile evolution of silicon oxide using a Cr hard mask and we extend our previous investigation by performing detailed and systematic analysis to gain a better insight of the effect of each parameter on the overall etching process. To this aim, we conduct a series of experiments in which we tune one parameter at a time, while the others are kept at the optimized values of the standard recipe,[226] with the focus on high fidelity transfer and vertical sidewalls fabrication. Our main findings are: *i)* an intermediate temperature (T=-10˚C) allows for slow deposition rates, directional transfer (and therefore vertical sidewalls) and flat bottom surfaces; *ii)* the profile is further improved by working at very low pressure (p=5mTorr), since the ion energy is higher and the concentration of the radical is low, which makes the anisotropic etching by Ar ions the dominant process and leads to vertical features with limited undercut; and *iii)* higher forward bias power (P_{Bias}=4W) significantly increases the directionality of the ion bombardment and therefore improves the verticality of the etching profile. Combining the best parameters into one process, we demonstrate the achievement of high fidelity transfer and aspect ratio independent etching (ARIE) via ALE, with features exhibiting average undercut values as low as 3.7±0.5% for five trench sizes, from 150nm to 30nm, as well as average sidewall angle of 87˚±1.5˚, very close to the 90˚ value of an ideal, perpendicular wall.

6.2 Profile evolution of SiO_2 features

6.2.1 Cr mask patterning

For the patterning of the Cr hard mask, a lift-off process has been used. First, nano-sized lines are created on poly(methyl methacrylate) (PMMA) using electron-beam lithography (Vistec VB300) on wafers with Si substrates with 250nm of thermally grown SiO_2. The PMMA thickness is 60nm and the line width varies from 30 to 200 nm. Next, a 12nm Chromium (Cr) layer at a pressure of 2×10^{-6} Torr is formed using e-beam evaporation. A final lift-off process with Remover PG (MicroChem) followed by acetone cleaning in an ultrasonic bath is used to define the Cr lines.

6.2.2 Atomic layer etching process details

Atomic layer etching is carried out in a conventional Plasmalab System 100 inductively coupled plasma (ICP) etcher from Oxford Instruments Plasma Technology with liquid nitrogen cryogenically cooled staged. Forward RF power (13.56 MHz) is applied to the substrate electrode to accelerate ions toward the substrate. The samples are cut and bonded onto 4 inches Silicon carried wafers using Fomblin oil, which improves the thermal contact between the sample and the carrier.

Figure 6.1 shows a schematic ALE process sequence. Ar gas flows continuously at 100 sccm during the entire process. The ICP power is held constant at 300 W, which creates a steady state Ar plasma for the entire length of the process. For the deposition half-cycles, short periodical injections of 10 sccm of CHF_3 are introduced. The injection time is 3 s to ensure a stable and reproducible FC injection. After the CHF_3 pulse, a purging step of 30 s with pure Ar plasma ensures that all the FC compounds are exhausted from the process chamber. The forward bias power supplied by the substrate electrode generates a direct current (DC) bias that controls the ion energy at the substrate. The deposition and purge steps are unbiased (DC bias=0 V). During the etch half-cycle, forward RF power is applied (P_{Bias}=2 – 4 W) to generate a DC bias in the range of -9 – -19 V. The etch step length is fixed at 60 s. Forward bias power (DC bias), pressure, and substrate temperature are varied to investigate a wide range of parameters. Etched samples are imaged in a Zeiss Ultra 60 scanning electron microscope (SEM) to determine the SiO_2 profile and depth. FC polymer deposition is also measured on blank SiO_2 wafers using a UVISEL spectroscopic ellipsometer from Horiba.

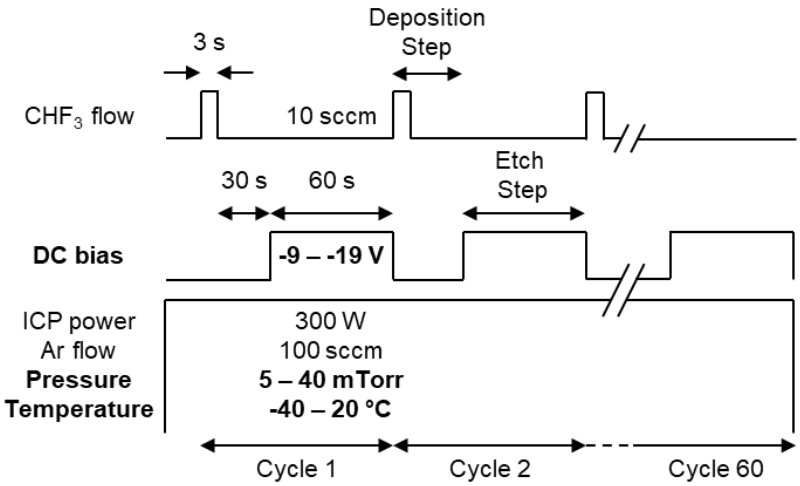

Figure 6.1 Schematic of the cyclic ALE process used, consisting of a repeating deposition step and etch step. The process parameters which we vary are the substrate temperature, the forward bias power, and the process pressure.

The ion energy distribution (IED) of the plasma is measured using a commercial retarding field energy analyzer (RFEA) Semion™ System 500.[217, 218] IED are collected as a function of the pressure, using pure Ar plasma with 300 W inductively coupled source power and 2 W forward bias power.

6.3 Results and Discussion

This Chapter aims to target the optimization of the SiO_2 etching profile for nanoscale-sized features (30-200 nm) by means of investigating the effect of such parameters as the temperature, pressure and forward bias power on the etched profiles.

We then evaluate their impact on the etched features by comparing key profile parameters, namely: the sidewall angle (ϑ), the undercut, and the etching rate per cycle (EPC, Å/cycles), as depicted in Figure 6.2. The sidewall angle ϑ describes the deviation from an ideal, perpendicular sidewall and is defined as the angle that the lateral wall forms with the plane tangent to the surface, with 0° being parallel to such surface and 90° representing the ideal, perpendicular sidewall. The undercut percentage measures the amount of SiO_2 that has been removed from the region underlying the Cr mask, thus introducing a deviation from the ideal pattern transfer and causing the lateral walls to form the sidewall angle ϑ.

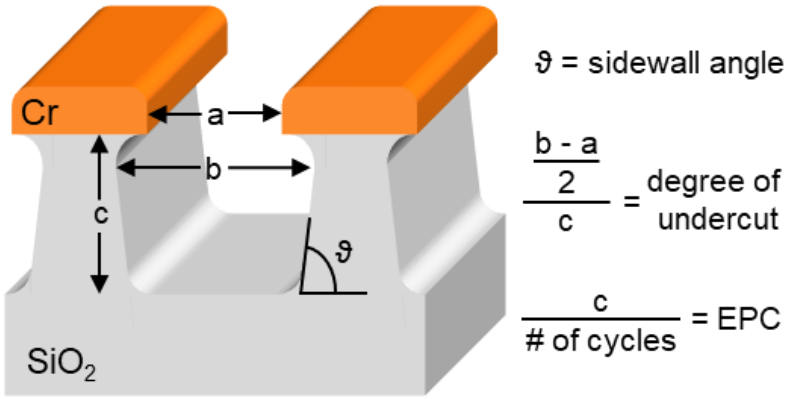

Figure 6.2 Schematic cross-section of samples used in this work with features parameter definition: sidewall angle, degree of undercut, etching per cycle (EPC).

We calculate the percentage degree of undercut as $\frac{(b-a)/2}{c}$ (100 %), i.e., the difference between the widest (b) and narrowest (a) widths of the feature after etching is completed, normalized to the thickness of the SiO_2 etched feature (c). An undercut close to 0 and a sidewall angle reaching 90° describe the achievement of high fidelity pattern transfer. Finally, we define the etching depth of each cycle (EPC, Å/cycle) as the thickness of the SiO_2 etched feature (c) divided by the total number of cycles, which is 60 for all the etching processes reported in this Chapter.

We measure and report these parameters (sidewall angle, undercut and EPC) as a function of the substrate temperature, the process pressure and the forward bias power. The plotted trends consist of the average values between different trench sizes (30, 40, 50, 100, 150, 200 nm), with the respective error bars computed as the standard deviation from each average.

6.3.1 Effect of the substrate temperature on ALE mechanism

We start our investigation with a detailed analysis of the temperature effect on the SiO_2 etch profile, reported in Figure 6.3. As noticed in Chapter 5,[226] the substrate temperature has a non-negligible impact on the ALE performances, since it strongly affects the sticking coefficient of the deposited FC polymer and therefore the overall ALE process.[227] In addition, the temperature also has a significant effect on the chemical etching caused by fluorine in the chamber.

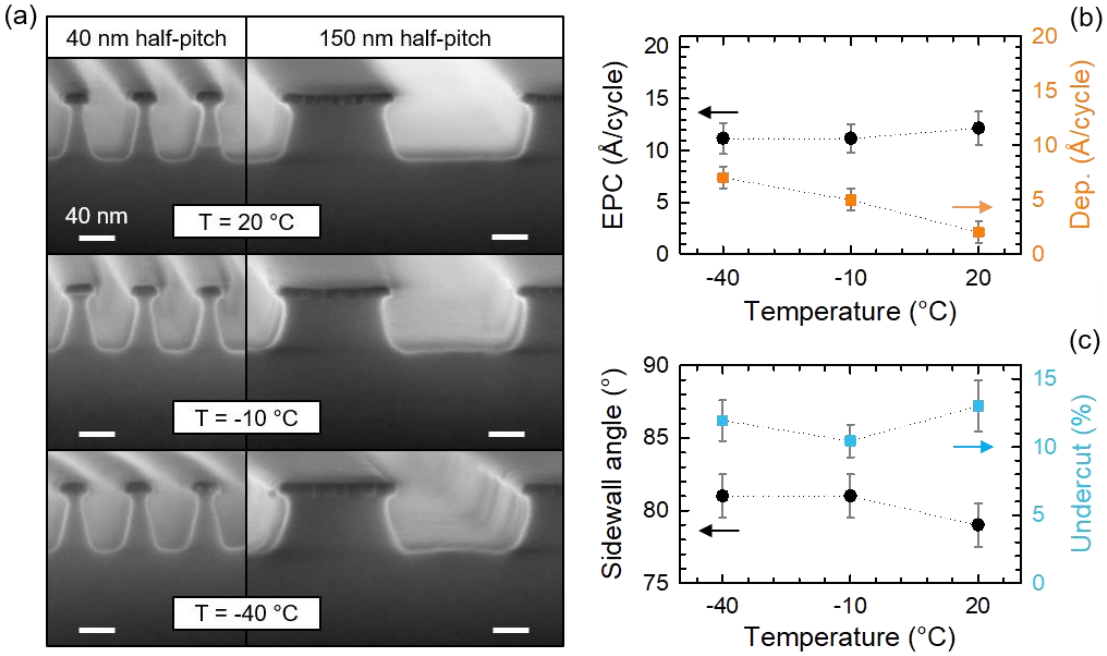

Figure 6.3 (a) Cross-sectional SEM images of silicon oxide features patterned using FC-Ar ALE, reported for three different processing temperatures, namely: T=20˚C (top panel), T=-10˚C (center), T=-40˚C (bottom panel). Two different trench sizes are shown: 40nm and 150nm. Both features for each temperature are obtained after 60 ALE. The scale bar is 40nm for all panels. (b) Etched silicon oxide thickness per cycle (EPC, Å/cycle, black dots, left axis) and fluorocarbon film thickness per cycle (orange squares, right axis) deposited onto the SiO_2 during one ALE cycle. Both are reported as a function of the substrate temperature during the process. (c) Sidewall angle (black dots, left axis) and degree of undercut (blue squares, right axis) as a function of the substrate temperature.

When the substrate temperatures are higher than T=−10 ˚C, the etching rate increases, due to residual fluorine radicals coming from the chamber wall. Moreover, higher temperatures (T=-10˚C – +20˚C) enhance SiO_2 chemical etching by fluorine, generating an undesired reaction between the FC polymer and the SiO_2 surface during each ALE cycle.[221] Increasing the chemical reaction between SiO_2 and FC results in higher etch rate, but at the expense of the film integrity and etch selectivity for SiO_2 over other materials.[187, 228, 229] However, while we demonstrated that ALE at T=-10˚C ensures self-limiting behavior and aspect ratio independent etching,[222, 224, 226] to date, no study has been reported on the temperature effect on the ALE patterning of silicon oxide.

Here, we perform ALE at three different temperatures: T=-40, -10, and +20 ˚C. Figure 6.3(a) shows the corresponding SEM pictures for 40nm and 150nm trenches. We kept the pressure and forward bias power at fixed values, respectively, p=10mTorr and P_{Bias}=2W,

which corresponds to a DC bias of -9V. EPC, sidewall angle and undercut are displayed in Figure 6.3(b) and Figure 6.3(c). Although the EPC remains constant throughout the investigated temperature range, the deposition per cycle drops from 7 Å/cycle at T=-40°C to 3 Å/cycle at T=+20°C. The detrimental effect of a higher FC deposition rate is particularly evident by looking at the bottom of the 150nm features. Such round surface becomes more and more flat with increasing temperatures, as can be appreciated in the flat bottom of the same size feature (150nm) for T=+20°C. Moreover, the bottom of the features obtained at T=-40°C also exhibits increased roughness, which indicates incomplete removal of the FC polymer. This effect stems from the fact that the lower temperature leads to thicker FC films, which requires longer etching steps in order to completely remove both the FC and mixed layer. On the other hand, the flat surface obtained at T=+20°C is accompanied by a higher undercut value and a more inclined sidewall (see data in Figure 6.3(c)), whereas such values are slightly improved for substrate temperature of T=-10°C. As a result, we identify the latter value as the best compromise within the probed temperature range between a slow deposition rate and an optimal directional transfer, in order to obtain improvements in both flat bottom surfaces and vertical features.

Importantly, our data allows us to draw important conclusions on the ALE mechanism. We show that ALE etching of SiO_2 strongly depends on the synergy between the accelerated Ar ions and the FC layer, while being softly sensitive to the range of temperatures we explore (T=-40 – +20°C). Hence, ALE does not operate as a thermally activated process, but rather finds its dominant driving force in a combination of chemical and kinetic processes between the accelerated ions and the mixed layer.

6.3.2 Effect of the pressure and ion energy distribution

Pressure is another pivotal parameter in ALE, since it directly affects the Ar ions flux and energy, as well as the concentration of Ar, C, and F radicals in the plasma. In order to study the effect of pressure alone, we maintain a fixed substrate temperature of T=-10°C and forward bias power at P_{Bias}=2W (DC bias of -9V) and we change the pressure level from p=5mTorr, to p=10, 25 and 40mTorr to conduct the ALE process, as reported in Figure 6.4(a). During each experiment, the pressure is kept constant thanks to the automatic pressure controller of our Plasmalab System 100 ICP.

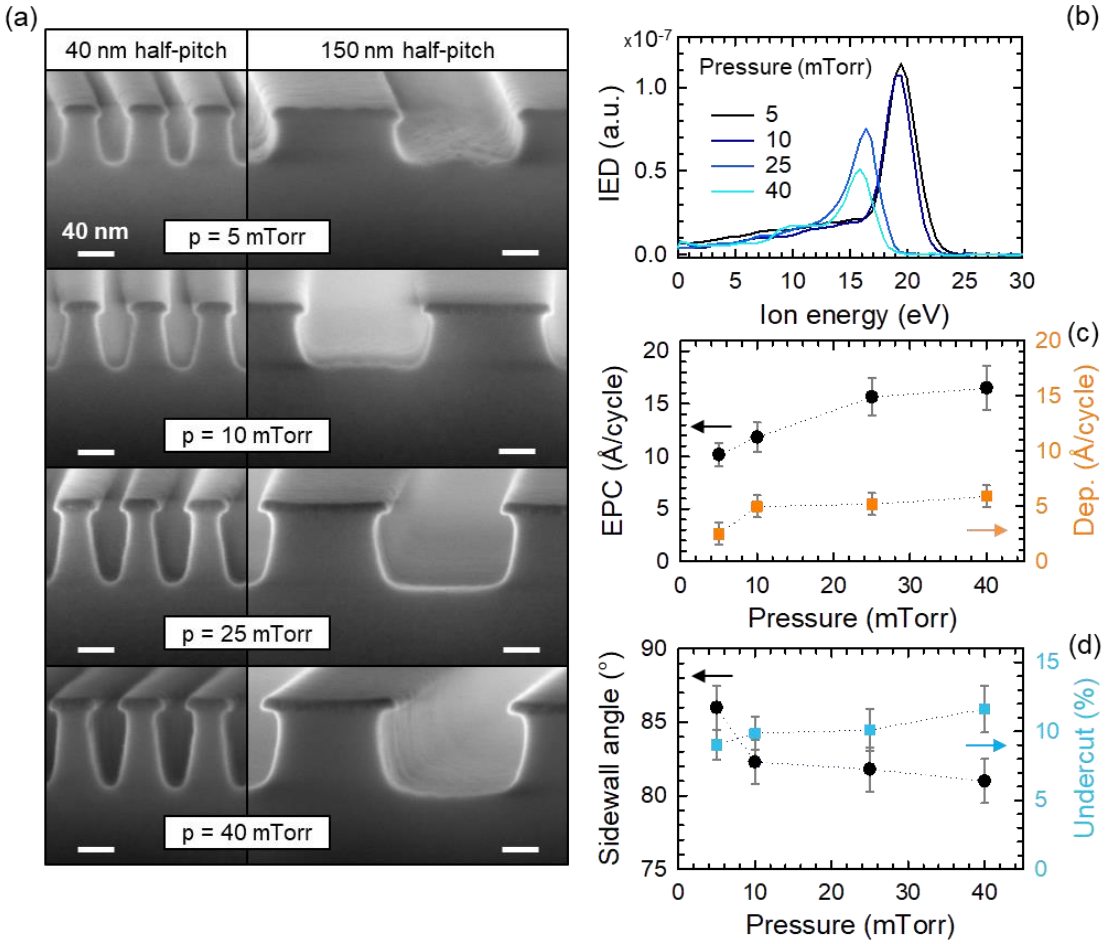

Figure 6.4 (a) Cross-sectional SEM images of silicon oxide features patterned using FC-Ar ALE reported for four different pressure values, p=5mTorr, 10mTorr, 25mTorr and 40mTorr. Two different trench sizes are shown: 40nm and 150nm. Both features for each pressure value are obtained after 60 ALE cycles. The scale bar is 40nm for all panels. (b) Ion energy distribution (IED) for each pressure value as in (a). The experimental parameters used to measure the IED are -9 V DC bias, 300 W ICP power and 100 sccm Ar flow. (c) Etched silicon oxide thickness per cycle (EPC, Å/cycle, black dots, left axis) and fluorocarbon film thickness per cycle (orange squares, right axis) deposited onto the SiO_2 during one ALE cycle. Both are reported as a function of the pressure values reported in (a). (d) Sidewall angle (black dots, left axis) and degree of undercut (blue squares, right axis) as a function of the pressure values in (a).

In order to gain better insight into the process mechanisms, for each pressure level we carefully characterize the ion energy distribution (IED) of the Ar plasma, as shown in Figure 6.4(b). The IED for the lowest pressure values (namely, p=5mTorr and p=10mTorr) exhibits a single peaked energy distribution. Such a distinct peak corresponds to the average energy that the ions gain while traveling across the plasma sheath.[218] When the

chamber pressure increases, the mean free path of the ions becomes shorter than the plasma sheath width. As a result, the ions will no longer travel ballistically through the sheath, but will experience collisions with neutral gas molecules and radicals before striking the electrode. The collisions with the neutrally-charged particles cause ions to lose energy, which results in the IED shifting to lower values (see Figure 6.4(b) for p=25mTorr and p=40mTorr).[230]

The different IEDs at the various pressure levels directly affect the etching features. For instance, at low pressure (p=5mTorr) the F and C radical densities are relatively low[231], while the ion energy is the highest between the investigated pressure levels. As a result, the etching results into an anisotropic-like etching with a reduced EPC (see Figure 6.4(c)) and a steep sidewall (86°) (Figure 6.4(d)). On the other hand, the SEM pictures (Figure 6.4(a), 150nm half-pitch, p=5mTorr) highlight an increased roughness at the bottom of the trench, suggesting that the FC film cannot be completely removed by the ions during the etch step. In order to confirm this hypothesis, we perform additional experimentation with the same parameters but longer etch steps, i.e., the time interval has been increased from t_{etch}=60 s to t_{etch}=180s. As reported in Figure 6.5, a longer etching time indeed allows for a complete removal of the polymer and leads to a flat bottom surface.

When the pressure increases, more radicals become available from the plasma system, and the etch rate grows by over 60% from a chamber pressure of p=5mTorr to p=40mTorr. Concurrently, the features become more tapered and show a larger local bowing. The etching rate trend hints to the fact that at higher pressure we are working in a chemical-reaction limited regime, as opposed to a physical-reaction limited where the etch rate would decrease. The monotonic growth of the undercut confirms the chemical-limited regime, since an increased undercut is due to chemical etching by the F radicals. Finally, we note that the sidewall angle decreases with pressure with the best result obtained at p=5mTorr with an 86° angle. This is a further confirmation that a lower pressure enables anisotropic etching thanks to the combined effect of high ion energy and a lower contribution to the isotropic etching by the F radicals at a low concentration.

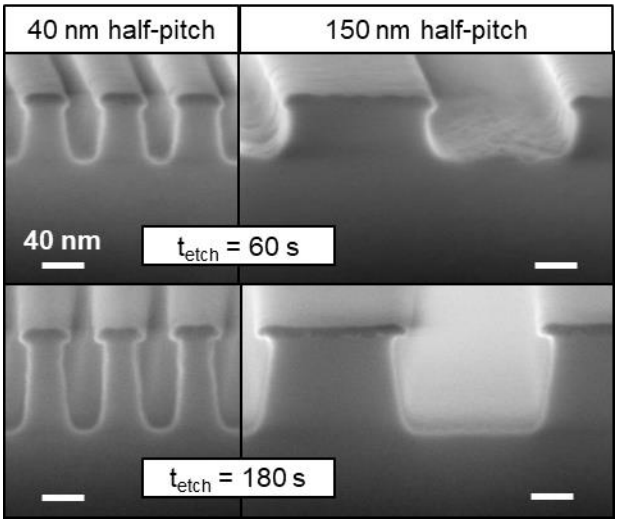

Figure 6.5 Cross-sectional SEM images of silicon oxide features patterned using FC-Ar ALE reported for two different etch times: tetch=60s and tetch=180s. Two different trench sizes are shown: 40nm and 150nm. Both features for each pressure value are obtained after 60 ALE cycles. The scale bar is 40nm for all panels.

6.3.3 Effect of the bias power on the etching directionality

Finally, we examine the effect of the forward bias power and, consequently, of the DC bias on the etched profiles. All other parameters are kept constant, with a pressure of p=10mTorr and a temperature of T=-10°C, based on the best results of our previous study which we know ensure a self-limiting behavior and aspect-ratio independent etching.[226] The profile evolution of SiO_2 features is shown in Figure 6.6(a) for increasing forward DC bias applied during the etch step. In order to work inside the ALE process window, and avoid any sputtering of SiO_2 during the etch step, the maximum DC bias allowed is -19 V.[62, 226]

Figure 6.6(b) shows the EPC as a function of the increasing bias, which corresponds to an increase in the forward bias power from P_{Bias}=2W (DC_{bias}=-9V) to P_{Bias}=3W (DC_{bias}=-12V) and P_{Bias}=4W (DC_{bias}=-19V). The deposition per cycle is not reported since it is a constant value of 5 Å/cycle for all the applied bias. Indeed, the FC deposition step in the ALE process is independent from the power applied during the etch step. Following the increase of the forward power, the Ar ion energy distribution shifts to larger values.[5, 223] As a result, ions with a higher energy interact with the mixed layer during the etch step, which leads to a deeper SiO_2 etching and higher EPC. Lower forward biases and therefore lower Ar ion energies have the undesired effect of needing a longer time to completely remove the FC layer, causing an incomplete removal of the mixed layer at the bottom of the feature.

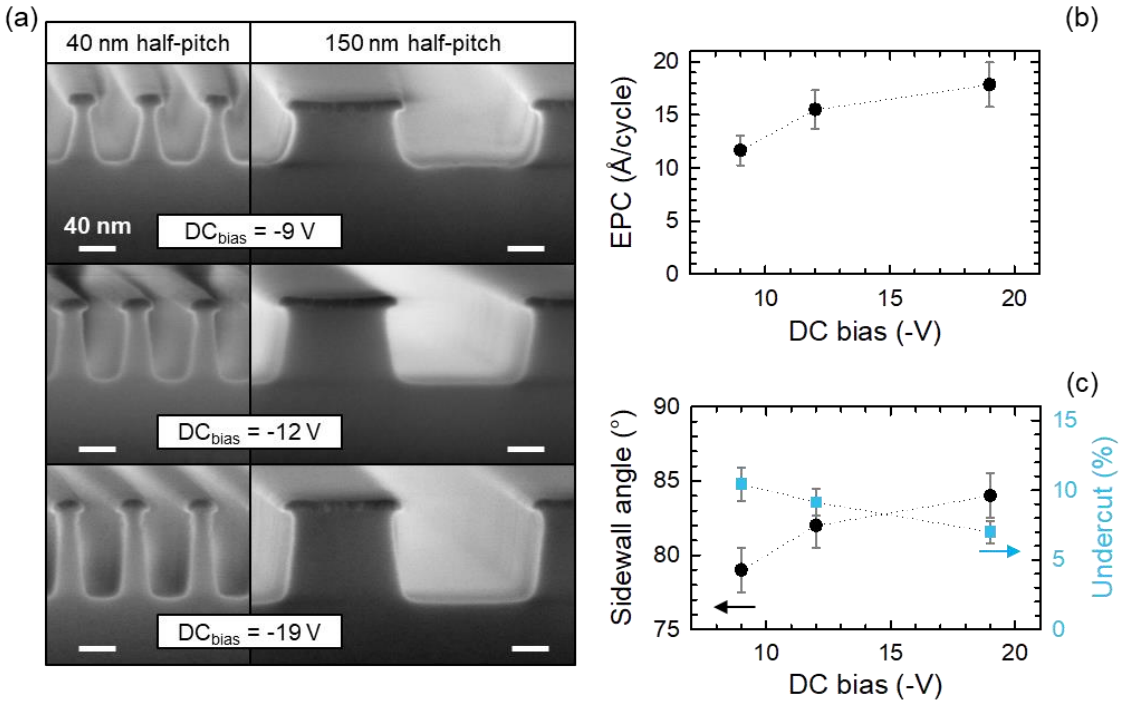

Figure 6.6 (a) Cross-sectional SEM images of silicon oxide features patterned using FC-Ar ALE reported for three different forward bias power, namely: P = 2W, 3W and 4W, corresponding to an applied DC bias of -9V, -12V and -19V. Two different trench sizes are shown: 40nm and 150nm. Both features for each DC bias are obtained after 60 ALE cycles. The scale bar is 40nm for all panels. (b) Etched silicon oxide thickness per cycle (EPC, Å/cycle, black dots) as a function of the same negative DC bias values reported in (a). (c) Sidewall angle (black dots, left axis) and degree of undercut (blue squares, right axis) as a function of the negative DC bias as in (a).

Another consequence of the increasing forward power is that more ions are incident on the electrode with a smaller deflection angle due to the smaller contribution of the ion-neutral scattering at higher energies.[232] This effect is appreciated in the sidewall angle and undercut trends shown in Figure 6.6(c): the profiles become more vertical, with the angle increasing from 78° at -9V DC bias to 85° at -19 V DC bias and the undercut dropping from 10% down to 6% for the same DC bias values, respectively.

We therefore reach the important conclusion that an increase in the forward power improves the overall feature shape, since it allows for a more anisotropic etching. In this case, the competition between FC deposition and ion bombardment leads to more vertical feature walls, a limited undercut and a flat bottom of the features, therefore balancing the

deposition and the etch step within one ALE cycle. We identify -19 V DC bias (corresponding to P_{Bias}=4W) as the optimum value to use in future pattering design of SiO_2.

6.3.4 Aspect ratio independent etching

Figure 6.7 (a)–(e) shows a series of Cr masked SiO_2 features with different trench sizes, etched for 60 ALE cycles under the optimal ALE self-limiting conditions that we have gathered throughout this chapter for obtaining flat surfaces, namely: T=−10°C, p=5mTorr, DC bias=-19 V, t_{etch}=60s. Previously (Figure 6.5), we show that for a pressure of 5 mTorr and DC bias=-9 V an etch time of 180s is needed for completely removing the FC polymer. However, using a higher DC bias of -19V allows for complete removal of the polymer after 60s. Notably, all features exhibit the same vertical profile, with an average value of 87°±1.5°, very close to a perfectly perpendicular wall (90°), as well as a low undercut of 3.7±0.5%, which demonstrate that our process allows for achieving ARIE in a conventional ICP tool.

Therefore, features with large aspect ratios etch as fast as those with low aspect ratio, regardless of the feature width. A slight undercut beneath the mask can still be observed, and can be ascribed to chemical and/or kinetic processes, such as ions and radicals reflected from the edges of the feature, broad Ar ions angular distribution, or residual fluorine from the chamber wall.[224] Conversely, we can rule out the contribution of ions scattered from the feature edges, since the sidewall profile does not change significantly with the feature width.

On the basis of Chapter 5 and 6, we can conclude that the main cause of the undercut is coming from the fluorine radicals in the chamber. Our study therefore highlights that, in order to achieve features without any undercut and thus a complete ALE, it is paramount to find a careful balance between the Ar ion parameters (i.e., energy and angular distribution) and the FC chemical reactants.

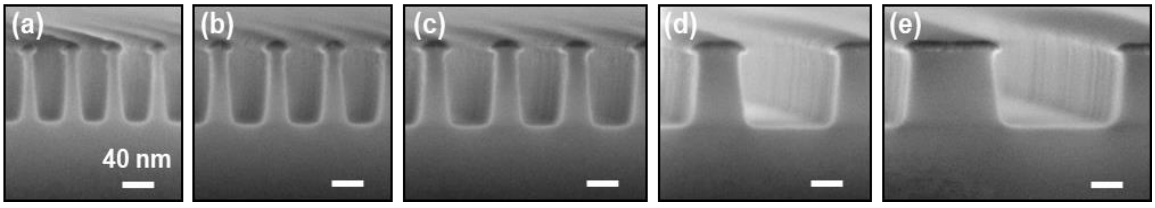

Figure 6.7 (a–e) Cross-sectional SEM images of silicon oxide features patterned using FC-Ar ALE. Different trench sizes after 60 ALE cycles: 30, 40, 50, 100, 150 nm from (a) to (e). Experimental parameters are T =-10˚C, p=5mTorr, DC bias=-19V, ICP power 300W. The scale bar is 40 nm for all panels.

6.4 Summary and Conclusions

In this chapter, we extensively study and characterize a cyclic CHF_3/Ar ALE process using a conventional ICP tool. We investigate the effect that the main process parameters, namely, the substrate temperature, chamber pressure, and bias power, have on the etching of 30 – 150 nm features into SiO_2, in order to gain better insight into the ALE mechanism while simultaneously finding the best conditions for the ALE process.

We find that the investigated temperature range (T=-40 – +20˚C) does not have a significant effect on the ALE behavior, which helps us to draw the important conclusion that the ALE is not a thermally activated process, but rather is dominated by concurrent chemical and kinetic processes between the accelerated Ar ions and mixed layer. However, we can still identify T=-10˚C as the best compromise between a slow deposition rate and an ideal directional transfer, which allows the realization of features with both a flat bottom surface and vertical lateral walls.

Conversely, the pressure has a more significant impact on the process, thanks to its direct effect on the ion energy distribution. Low pressure values (p=5mTorr) result in high ion energy and low density of F and C radicals, whose isotropic contribution to the etching thus becomes negligible. Hence, the anisotropic etching from the Ar ions dominates and enables the achievement of a reduced EPC and steep sidewalls (up to 86˚). Such ideal, vertical features are counterbalanced by the negative effect of rough and round bottom surfaces, due to incomplete removal of the FC film at low pressure. However, we demonstrate that this issue can be easily overcome by increasing the etching time from t_{etch}=60 s to t_{etch}=180s or increasing the bias voltage, thus allowing us to achieve flat bottom surfaces at low pressure values.

Etching directionality is also directly affected by the forward bias power, as shown through the exploration of three different bias powers (P_{Bias} =2, 3, 4W, corresponding to DC bias of -9, -12, -19V). In this case, a higher forward power leads to an increase in the ion energy distribution and smaller deflection angle, which translates into a deeper etching, complete removal of the FC layer and improved verticality of the etched features thanks to the dominant contribution of anisotropic over isotropic etching.

Combining the best parameters values that we find from the analysis of each parameter alone, that is, intermediate temperature (T=-10˚C), low pressure (p=5mTorr) and high forward bias power (P_{Bias} =4W), we demonstrate the achievement of etched features with exceptionally low undercut values (down to an average of 3.7±0.5%, calculated from five features ranging from 150nm to 30nm), almost vertical sidewalls (87˚±1.5˚, very close to an ideal 90˚ perpendicular wall), flat bottom surfaces and, importantly, aspect-ratio independent etching, which is extremely important for the actual integration of the ALE approach into existing production lines. Moreover, besides providing a paradigm process to obtain ARIE, our study fulfills the goal of gaining some important insight into the plasma physics and the mechanisms that drive the ALE process. We find that, while the thermal activation is a negligible effect, the driving force during ALE pattern transfer is a finely tuned balance between the kinetic and chemical reactions between the Ar ions and the FC radicals.

Finally, we notice that an accurate understanding of how each plasma parameter affects the ALE process enables a qualitative, but reliable feedback control on the plasma itself, since we learned how the etched features and their sidewall angle, undercut degree, bottom surfaces carry information about whether they are generated by anisotropic/isotropic mechanisms (ions vs radicals) and either higher/lower temperature, pressure and bias power.

Conclusions and Future Work

In the terms of this work, two objectives were pursued and accomplished.

The first one was the creation of a master template, which allows the fabrication of bit patterned media with areal density beyond 2 Tb/in^2. The developed master template has features made with titanium dioxide with critical dimensions of 7.5nm fabricated using spacer-defined double patterning (SSDP). Double patterning at such small dimension is enabled using atomic layer deposition for spacer material fabrication. As a result of using atomic layer deposition, the spacer-defined double patterning yields to a scalable process for the fabrication of single-digit nanometer feature sizes.

For the fabrication of 7.5nm features, the developed method employs a combination of self-assembled block copolymer and spacer defined double patterning. Atomic Layer Deposition (ALD) allows handling process limitations raising from the fabrication of sub-10nm half-pitch pattern. First, high pressure Al_xO_y ALD is used to selective sequential infiltration synthesis (SIS) of the oxide in the PS-*b*-PMMA block polymer. Chapter 3 shows the demonstration of Al_xO_y infiltrated PMMA 15nm half-pitch lines. During SIS, the vapors from an ALD process diffuse inside the block-copolymer polymer and selectively bind to the carbonyl groups in PMMA. Such selective infiltration of aluminum oxide in PMMA creates a hard mask suitable for high selectivity pattern transfer. Indeed, the fabrication of 15nm carbon mandrel lines is enabled by the fabrication of 15nm PMMA selectively infiltrated lines. SIS has the benefit of reducing line-edge-roughness of the BCP pattern. In addition, this work addresses the challenge of finding the window where the infiltration reaction occurs only within one block and produces features of the correct width.

In Spacer Defined Double Patterning a highly conformal spacer layer is deposited onto a sacrificial mandrel pattern. It has been shown that for a successful SDDP integration,

the performance of the spacer technology is a key parameter. ALD is particularly appropriate for the spacer fabrication because allows the formation of ultra-thin films with angstrom-level resolution by cyclical oxidation of a metalorganic precursor. Here, ALD parameters are studied and controlled for defining the feature size and frequency of the double patterned lines. Using spectroscopic ellipsometry, the performance of the spacer material on flat substrates is studied. Such study is extremely useful to understand the impact of spacer deposition on mandrel lines. It has been shown that plasma assisted ALD is not suitable for spacer fabrication. Indeed, high reactivity plasmas damage the underneath material. Radicals coming from O_2 plasma etch or modify the material where the spacer grows, affecting SDDP result. On the other hand, nucleation of thermal TiO_2 on different substrates does not show any etching. Overall, the TiO_2 thermal process was the best process identified and used as the spacer fabrication step during the SDDP process. In the end, 7.5nm robust standing lines are fabricated using DSSP. The resulting lines are not subject to pattern collapse, but exhibit a slight tilt.

In conclusion, spacer defined double patterning enables sub-10nm feature size transfer over large areas. This type of process enables scalable fabrication of single digit nanometer feature sizes for patterned media at densities beyond 5Tb/in^2. In addition, the achievements rising from this study on 7.5nm half-pitch feature fabrication can be extended to the semiconductor industry in integrated circuits fabrication.

Through the overall process demonstration we noted future challenges to be addressed particularly in the spacer etch and trim. This step should be optimized to produce a more vertical feature shape, reduce line edge roughness, and create the ideal spacer size for uniformly spaced double patterned features. Indeed, to minimize the tilt of the 7.5nm TiO_2 features, the carbon trim will need to be optimized to reduce any footing at the bottom of the feature. With optimization of the carbon trim step, the demonstrated process promises a route to enable sub-10nm features sizes transferable to a substrate for templates at density beyond 5Tb/in^2. The next steps in BPM master template fabrication are to transfer the TiO_2 pattern into the underlying chromium and then into the quartz template. Upcoming work will show our ability to control the chromium hardmask patterning with a TiO_2 mask using cryogenic temperatures during the chromium etching step. Notably, it is possible to take advantage of the wafer stack using during SDDP and extend the implementation of this method using any substrates compatible to chromium deposition.

The major contribution of the second part of this work is the experimental demonstration of fluorocarbon-based (FC) atomic layer etching (ALE) of SiO_2 using an approach that had first been theoretically examined. The work is in excellent agreement with computational predictions, demonstrating the power of coupling computational simulations and experiments. This process is further characterized in terms of plasma and process parameters. Fundamental aspects of ALE of SiO_2, in particular surface mechanisms, have been explored. Key mechanisms are characterized in order to enable a highly selective process design. This ALE approach is a very sensitive process. The FC deposition thickness per cycle is of the order of a few Ångstrom, and maximum ion energies range from 20 to 30 eV. Despite these relatively small changes in processing parameters, a significant impact on the etch behavior can be seen. During this study, it has become clear that highly controlled process parameters and chamber conditions are essential to maintaining high precision and etch control for ALE.

In chapter 4, a cyclic FC-based ALE approach was established for precise removal of SiO_2. The cyclic approach consists of a deposition step and subsequent etch step. During the deposition step, precise precursor injection allows for controlled FC film deposition on the order of several Ångstrom. After completion of the FC film deposition, a small bias potential is applied during the etch step. Low energy Ar^+ ion bombardment induces mixing of F with the SiO_2 substrate and removal of the FC film together with mixed, reacted substrate material. Once the chemical etchant is depleted, the etch rates decrease and self-limited material removal is observed. The thickness of the deposited FC film and ion energy can be used to precisely control the substrate removal per cycle. The process is consistent with simulations and first demonstration by Rauf *et al.,* Agarwal and Kushner, and Metzler *et al.*.[5, 52, 53, 203, 204]

The cyclic ALE process established in Chapter 4 was experimentally demonstrated in Chapter 5. To further characterize the process, plasma properties were measured in real-time during cyclic ALE. The precursor injection was shown to have a strong, but short impact on electron temperature, electron density, and plasma potential, consistent with continuous precursor admixtures. ALE of SiO_2 is further explored and characterized. The main process parameters investigated were the FC film thickness deposited per cycle, the maximum ion energy, and the etch step length. The FC film thickness deposited per cycle does yield a strong control over etch depth per cycle, the ion energy and etch step length, however, proved to impact material etching selectivity significantly. Lower ion energies

provide self-limiting SiO_2 etching aspect ratio independently. CHF_3 has a lower deposition yield than other FC gases and is here used as precursors. Using ellipsometry, we studied the SiO_2 etch per cycle relative to the etch step time as a function of substrate temperature. At -10 ˚C the contributions to chemical etching coming from fluorine radicals and fluorocarbon compounds from the chamber walls are minimized and a quasi-self-limiting behavior ALE is observed after 60 s etch time. However, deviation from self-liming ALE behavior clearly indicates the presence of a secondary supply of fluorine from the chamber walls. Additionally, during the initial stages of the etch, the fluorocarbon film buildup over multiple ALE cycles causes an increase in EPC with the number of ALE cycles.

In chapter 6, the cyclic ALE approach, successfully developed, was used for etching of 30 – 150 nm features into SiO_2. The effect of the main process parameters, namely, the substrate temperature, chamber pressure, and bias power were investigated. While temperature does not have a significant effect on the ALE behavior for feature pattering, pressure and power strongly affect the etching. Using ALE at low pressure (p=5mTorr) and high forward bias power (P_{Bias} =4W), we demonstrate the achievement of etched features with exceptionally low undercut values (down to an average of 3.7±0.5%, calculated from five features ranging from 150nm to 30nm), almost vertical sidewalls (87˚±1.5˚, very close to an ideal 90˚ perpendicular wall), flat bottom surfaces and, importantly, aspect-ratio independent etching (ARIE), which is extremely important for the actual integration of the ALE approach into existing production lines. Moreover, besides providing a paradigm process to obtain ARIE, our study fulfills the goal of gaining some important insight into plasma physics and the mechanisms that drive the ALE process. We find that, while the thermal activation is a negligible effect, the driving force during ALE pattern transfer is a finely tuned balance between the kinetic and chemical reactions between the Ar^+ ions and the FC radicals.

In this work we have been able to demonstrate a novel approach to ALE, with high etching precision and pattern transfer fidelity. The understanding obtained will impact micro- and nanostructure fabrication in general, and thus impact other disciplines which utilize the results of these fabrication methods. Challenges and obstacles encountered during this work help clarify how to approach and solve these issues for scientific work at the nanometer scale. This work has found wide-spread interest in many other research groups and several companies already.

The understanding of the mechanisms of ALE of SiO_2 gained in this work can be used to optimize ALE of SiO_2 for a variety of potential applications. Several process parameters (e.g. ion energy, surface fluorination, etch step length, and substrate temperature) greatly influence the etch performance. We have established a fundamental understanding of these impacts and involved mechanisms.

This work has shown that the chemistry employed during ALE has a strong impact on etching mechanisms. A reaction of the SiO_2 substrate with the injected precursor was described in Appendix A. CHF_3 has been explored as one example precursor. However, in order to clearly distinguish the impact of H, additional studies are necessary.[233-235] Additionally, other chemistries are of great interest. A wide variety of FC precursors are commonly employed in industry, e.g. C_4F_8, CF_4, C_2F_6, C_3F_6, or C_4F_6. Each precursor shows different dissociation, deposition yield, and deposited FC film characteristics. The addition of oxygen, in the form of O_2 admixture or directly in the precursor molecule can yield potentially interesting results.

Next to varying the precursor injection, the carrier gas chemistry can be explored, too. Ion bombardment plays an essential role in this ALE approach. For the current work, low energy Ar^+ ions are employed. Other commonly employed carrier gases include He and N_2. The ion mass varies significantly between these three chemistries.

One of the limitations of ALE is slow processing rates and the resulting low wafer throughput. The current process consists of a FC film deposition and subsequent etch step. This separation allows great process control and dedicated characterization. In order to speed up processing, the possibility of eliminating a dedicated FC film deposition step can be explored. The process itself is based on similar principles. The Ar plasma would, in this case, be continuously biased. Periodic, precise precursor injections control and limit the amount of chemical reactant. Similar etch characteristics, are expected. Considering the current typical times of 33 s for a deposition step and 60 s for an etch step, cycle times could potentially be reduced by ≈50%.

Directionality is of key interest in the application of ALE. ALE ideally provides anisotropic etch behavior. Directionality is usually based on energetic ion bombardment. The low ion energies needed for successful ALE may suffer from reduced directionality.[236] The characterization of ALE of structures has been started in Chapter 6 and showed first

promising results. The effect of process parameters for cyclic etching on 3D structures is, however, not yet clear and can greatly differ from continuous etching. Further characterization, e.g. of tight pitch features and etch uniformity, is important for the potential implementation of ALE in manufacturing. A uniform deposition is necessary for a uniform etch. Feature size and aspect ratio can greatly influence FC sidewall deposition based on the line of sight of reactive species.[237, 238] This effect can lead to preferred deposition at the top of small features and ultimately to occlusion of these features. The uniformity of the cyclic deposition is of particular interest since it will greatly affect the subsequent etching.

The semiconductor processing industry is moving towards manipulating single layers of atoms. Critical dimensions have been shrinking, following Moore's Law, for decades.[238] Continuing the current trend will eventually lead to critical dimensions on the order of only several atoms or molecules, therefore setting a hard limit to scaling. In addition to this limit, heat dissipation becomes an increasing challenge in modern day processors. We believe that the understanding and knowledge gained with this work will help future studies on engineering at the Ångstrom scale.

Appendix A – Surface chemistry during Fluorocarbon-based atomic layer etching of SiO_2 with CHF_3 and Ar plasmas

1 Experimental apparatus

Surface chemistry measurements are run on SiO_2 samples processed with a full ALE cycle, with the etch step time ranging from 0 s up to 3 min. For this study, X-ray photoelectron spectroscopy (XPS) measurements are conducted in a K-Alpha$^+$™ spectrometer system from Thermo Scientific™. Samples are secured to a holder and loaded into the analysis chamber via a load-lock. Experiments are typically run at a vacuum pressure of ranging from $5x10^{-7}$ to $9x10^{-7}$ mbar. Monochromatic Al Kα x-rays are focused to a spot size of 100 μm on the sample surface at a beam current of 1.16 mA, and a dual-beam flood source consisting of very low energy ions and electrons is utilized for charge compensation.X-ray measurements consisted of survey spectra at 200 eV pass energy and 1 eV energy step size, scanned spectra in the valence binding energy region at 50 eV pass energy and 0.2 eV energy step size, and snapshot spectra of 15 frames in the C1s, and F1s binding energy regions taken at 1 second per frame at 149.6 eV pass energy with 128 energy channels.

Thermo Scientific™ Avantage software was used for all instrument control, data processing, and peak fitting. C1s spectra were fit using C–C, C–CF_x (x = 1, 2, and 3), CF, CF_2, and CF_3 peaks at 284.8 eV, 287.1 eV, 289.2 eV, 291.57 eV, and 293.78 eV, respectively, with a range of ±0.2 eV across all experiments.[239, 240] A typical decomposition of the C1s spectra into these fitted peaks is shown in Figure A.1. F1s spectra were fit using Si-F_x (x = 1, 2, and 3) and C-F_x (x = 1, 2, and 3) peaks at 687.9 eV and 688.9 eV, respectively, with a range of ±0.2

eV across all experiments.[241] A typical decomposition of the F1s spectra into these fitted peaks is shown in Figure A.2.

2 Silicon oxide surface chemistry during CHF_3-based ALE

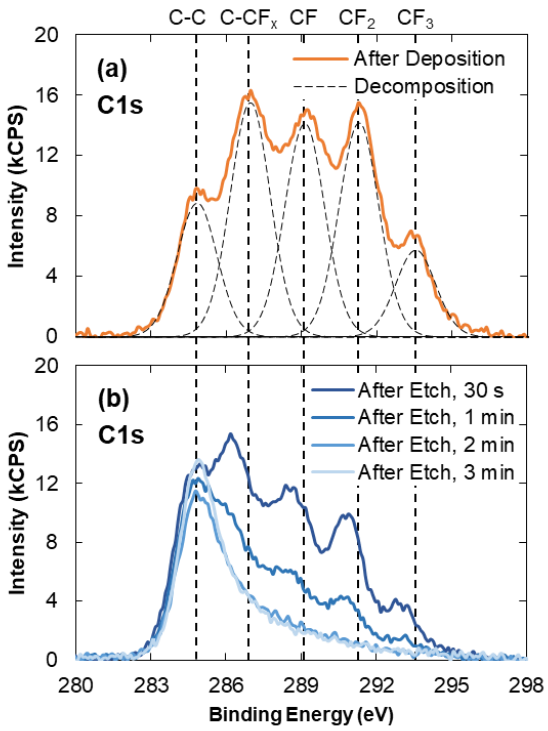

Figure A.1 C1s XPS spectra comparing the surface chemistry of the fluoropolymer and mixed layer interface at different stages of the ALE cycle. (a) After deposition of 5 Å of FC polymer. (b) After 30 seconds up to 3 minutes of etching. A decomposition of the spectra representing different degrees of fluorination in the carbon bonding is shown.

One ALE cycle was conducted on each sample with varying lengths of the etch step. The length of etching in these experiments ranged from 0 s (deposition only) up to 3 min. XPS measurements were then conducted on each sample to study the composition of the deposited polymer as well as the change in surface chemistry for varying lengths of the ALE etch step. It was found that the deposited polymer consists only of carbon and fluorine (Figure A.1(a)).

As the etch step is lengthened, the FC is etched more thoroughly, as can be seen by the reduction and/or disappearance of the C-CF_x, CF, CF_2, and CF_3 peaks in Figure A.1(b).

As the FC is etched, fluorine is preferentially removed and propagates through the FC to mix and react with the SiO_2 substrate. This is exemplified in Figure A.1(b) by the larger reduction of the CF_x compared to the C-C peak, which is in agreement with previous work from Metzler *et al.*[52, 204, 207] The source of C-C peak is a combination of the FC as well as surface contamination resulting from the transfer of the sample from the ICP etching system to the XPS.

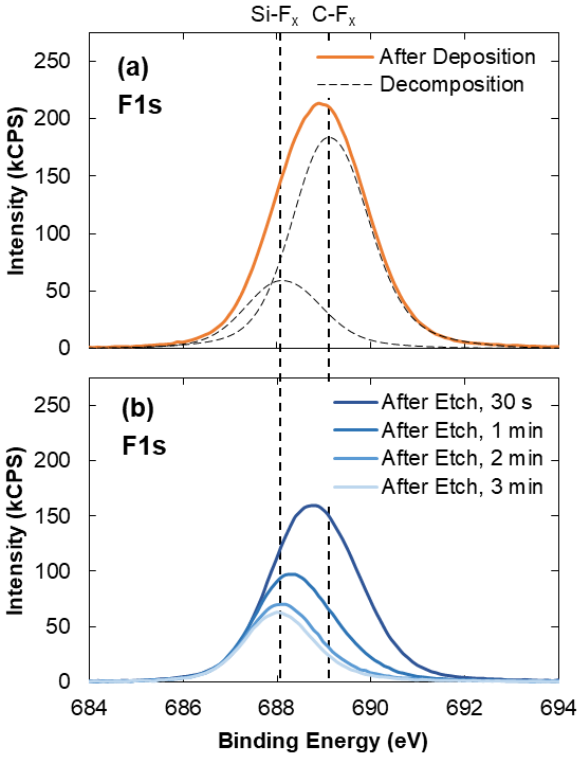

Figure A.2 F1s XPS spectra comparing the surface chemistry of the fluoropolymer and mixed layer interface at different stages of the ALE cycle. (a) After deposition of 5 Å of polymer. (b) After 30 seconds up to 3 minutes of etching. A decomposition of the spectra representing fluorine bonded to carbon in the polymer and to the SiO_2 substrate is shown.

Figure A.1(b) also shows that the difference between 1, 2 and 3 min of etching is negligible, indicating that the ALE etch step can be limited to 1 min. Most of this removal takes place within the first 60 s of ion bombardment as the C1s signal after 120 and 180 s of ion bombardment is comparable. The real time ellipsometry, shown in Figure 5.5, confirms this observation and shows only little change in the FC film thickness after 60 s of ion bombardment. Furthermore, a residual carbon film is seen in XPS at the end of the etch step, i.e., after 180 s of ion bombardment.

Figure A.2 shows the F1s spectra a shifting from 688.9 eV to 687.9 eV as the etch time increases from 0 s (After Deposition) to 180 s (After Etch, 3min). This shift indicates that the F1s spectra is a convolution of two peaks. This convolution is comprised of a C-F_x peak representing carbon-bonded fluorine in the polymer, and a Si-F_x peak representing silicon-bonded fluorine in the substrate. Figure A.2(a) shows F1s spectra after FC polymer deposition, which consists of 5 Å of FC layer on SiO_2. This spectra is a convolution of the C-F_x and Si-F_x peaks, which proves the formation of the fluorinated-SiO_2 layer (mixed layer) upon deposition of the FC.

As the etch step is lengthened, the C-F_x peak steadily disappears and the convolution in Figure A.2(b) begins to match the fitted Si-F_x peak from the after deposition sample. The consistency of the Si-F_x peak even after 3 min of etching is hypothesized to be a result of two potential phenomena. One explanation is that the Ar ions amorphized the surface of the SiO_2 and push fluorine down into the bulk substrate, making them less accessible for etching in a given cycle.[53] These entrapped ions are then measured in XPS even after the etching step is complete. The other possible explanation is the depletion of fluorine in an advancing reacted layer, meaning that as the FC and substrate material are being removed from the surface, residual fluorine is continuing to mix and react with the next layer of available SiO_2.[5, 242]

References

1. V. M. Donnelly and A. Kornblit, Plasma etching: Yesterday, today, and tomorrow, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **31** (5), 050825 (2013).
2. N. Marchack and J. P. Chang, Perspectives in nanoscale plasma etching: what are the ultimate limits?, *Journal of Physics D: Applied Physics* **44** (17), 174011 (2011).
3. C. G. Lee, K. J. Kanarik and R. A. Gottscho, The grand challenges of plasma etching: a manufacturing perspective, *Journal of Physics D: Applied Physics* **47** (27), 273001 (2014).
4. M. Leskelä and M. Ritala, Atomic layer deposition chemistry: recent developments and future challenges, *Angewandte Chemie International Edition* **42** (45), 5548-5554 (2003).
5. A. Agarwal and M. J. Kushner, Plasma atomic layer etching using conventional plasma equipment, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **27** (1), 37-50 (2009).
6. Y.-K. Choi, T.-J. King and C. Hu, Nanoscale CMOS spacer FinFET for the terabit era, *IEEE Electron Device Letters* **23** (1), 25-27 (2002).
7. G. Lansbergen, R. Rahman, C. Wellard, I. Woo, J. Caro, N. Collaert, S. Biesemans, G. Klimeck, L. Hollenberg and S. Rogge, Gate-induced quantum-confinement transition of a single dopant atom in a silicon FinFET, *Nature Physics* **4** (8), 656 (2008).
8. N. Singh, A. Agarwal, L. Bera, T. Liow, R. Yang, S. Rustagi, C. Tung, R. Kumar, G. Lo and N. Balasubramanian, High-performance fully depleted silicon nanowire (diameter/spl les/5 nm) gate-all-around CMOS devices, *IEEE Electron Device Letters* **27** (5), 383-386 (2006).
9. B. Yang, K. Buddharaju, S. Teo, N. Singh, G. Lo and D. Kwong, Vertical silicon-nanowire formation and gate-all-around MOSFET, *IEEE Electron Device Letters* **29** (7), 791-794 (2008).
10. C.-J. Su, T.-I. Tsai, Y.-L. Liou, Z.-M. Lin, H.-C. Lin and T.-S. Chao, Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels, *IEEE Electron Device Letters* **32** (4), 521-523 (2011).
11. C. T. Carver, J. J. Plombon, P. E. Romero, S. Suri, T. A. Tronic and R. B. Turkot, Atomic layer etching: An industry perspective, *ECS Journal of Solid State Science and Technology* **4** (6), N5005-N5009 (2015).
12. K. Eriguchi and K. Ono, Quantitative and comparative characterizations of plasma process-induced damage in advanced metal-oxide-semiconductor devices, *Journal of Physics D: Applied Physics* **41** (2), 024002 (2008).

13. T. Ivanov, M. A. Pourghaderi, D. Lin, J.-K. Yu, S. Tan, Y. Kimura, D. Hellin, J. Geypen, H. Bender and J. Vertommen, The influence of post-etch InGaAs fin profile on electrical performance, *Japanese Journal of Applied Physics* **53** (4S), 04EC20 (2014).

14. K. J. Kuhn, M. D. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, S. T. Ma, A. Maheshwari and S. Mudanai, Process technology variation, *IEEE Transactions on Electron Devices* **58** (8), 2197-2208 (2011).

15. G. Yuan, H. Li, B. Shan and J. Liu, Critical Atomic-level Processing Technologies: Remote Plasma-enhanced Atomic Layer Deposition and Atomic Layer Etching, *Micro and Nanosystems* **10** (2), 76-83 (2018).

16. K. J. Kanarik, T. Lill, E. A. Hudson, S. Sriraman, S. Tan, J. Marks, V. Vahedi and R. A. Gottscho, Overview of atomic layer etching in the semiconductor industry, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **33** (2), 020802 (2015).

17. H. Shimizu, K. Sakoda, T. Momose, M. Koshi and Y. Shimogaki, Hot-wire-assisted atomic layer deposition of a high quality cobalt film using cobaltocene: elementary reaction analysis on NH x radical formation, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **30** (1), 01A144 (2012).

18. S. Heil, Plasma-assisted atomic layer deposition of metal oxides and nitrides, (2008).

19. T. Suntola and J. Antson, (Google Patents, 1977).

20. M. N. Yoder, (Google Patents, 1988).

21. F. Djamdji and R. Blunt, Hall mobility profiling in high electron mobility transistor structures, *Materials Science and Engineering: B* **20** (1-2), 77-81 (1993).

22. Y. Horiike, T. Tanaka, M. Nakano, S. Iseda, H. Sakaue, A. Nagata, H. Shindo, S. Miyazaki and M. Hirose, Digital chemical vapor deposition and etching technologies for semiconductor processing, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **8** (3), 1844-1850 (1990).

23. G. N. Parsons, J. W. Elam, S. M. George, S. Haukka, H. Jeon, W. Kessels, M. Leskelä, P. Poodt, M. Ritala and S. M. Rossnagel, History of atomic layer deposition and its relationship with the American Vacuum Society, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **31** (5), 050818 (2013).

24. K. J. Kanarik, J. Marks, H. Singh, S. Tan, A. Kabansky, W. Yang, K. Taeseung, D. M. Hausmann and T. Lill, (Google Patents, 2017).

25. S. I. Association, International Technology Roadmap for Semiconductors 2005 Edition, http://www.itrs.net/, (2006).

26. O. Sneh, R. B. Clark-Phelps, A. R. Londergan, J. Winkler and T. E. Seidel, Thin film atomic layer deposition equipment for semiconductor processing, *Thin Solid Films* **402** (1-2), 248-261 (2002).

27. W. Lu, Y. Lee, J. Murdzek, J. Gertsch, A. Vardi, L. Kong, S. M. George and J. A. del Alamo, presented at the 2018 IEEE International Electron Devices Meeting (IEDM), 2018 (unpublished).

28. A. Paranjpe, S. Gopinath, T. Omstead and R. Bubber, Atomic layer deposition of AlO x for thin film head gap applications, *Journal of the Electrochemical Society* **148** (9), G465-G471 (2001).

29. A. M. Schwartzberg and D. Olynick, Complex materials by atomic layer deposition, *Advanced Materials* **27** (38), 5778-5784 (2015).

30. S. M. George, Atomic layer deposition: an overview, *Chemical Reviews* **110** (1), 111-131 (2009).

31. S. George, O. Sneh, A. Dillon, M. Wise, A. Ott, L. Okada and J. Way, Atomic layer controlled deposition of SiO2 and Al2O3 using ABAB… binary reaction sequence chemistry, *Applied Surface Science* **82**, 460-467 (1994).

32. A. Dillon, A. Ott, J. Way and S. George, Surface chemistry of Al2O3 deposition using Al (CH3) 3 and H2O in a binary reaction sequence, *Surface Science* **322** (1-3), 230-242 (1995).

33. O. Sneh, M. Wise, A. Ott, L. Okada and S. George, Atomic layer growth of SiO2 on Si (100) using SiCl4 and H2O in a binary reaction sequence, *Surface Science* **334** (1-3), 135-152 (1995).

34. M. Groner, J. Elam, F. Fabreguette and S. M. George, Electrical characterization of thin Al2O3 films grown by atomic layer deposition on silicon and various metal substrates, *Thin Solid Films* **413** (1-2), 186-197 (2002).

35. H. Lee and S. Bent, (Wiley, 2012).

36. X. Jiang and S. F. Bent, Area-selective ALD with soft lithographic methods: using self-assembled monolayers to direct film deposition, *The Journal of Physical Chemistry C* **113** (41), 17613-17625 (2009).

37. E. Langereis, S. Heil, H. Knoops, W. Keuning, M. Van de Sanden and W. Kessels, In situ spectroscopic ellipsometry as a versatile tool for studying atomic layer deposition, *Journal of Physics D: Applied Physics* **42** (7), 073001 (2009).

38. J. Klaus, A. Ott, J. Johnson and S. George, Atomic layer controlled growth of SiO 2 films using binary reaction sequence chemistry, *Applied Physics Letters* **70** (9), 1092-1094 (1997).

39. D. Schmidt, S. Strehle, M. Albert, W. Hentsch and J. Bartha, Top injection reactor tool with in situ spectroscopic ellipsometry for growth and characterization of ALD thin films, *Microelectronic Engineering* **85** (3), 527-533 (2008).

40. R. L. Puurunen, Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process, *Journal of Applied Physics* **97** (12), 9 (2005).

41. J. K. Kim, S. I. Cho, S. H. Lee, C. K. Kim, K. S. Min and G. Y. Yeom, Atomic layer etching removal of damaged layers in a contact hole for low sheet resistance, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **31** (6), 061302 (2013).

42. T. Matsuura, J. Murota, Y. Sawada and T. Ohmi, Self-limited layer-by-layer etching of Si by alternated chlorine adsorption and Ar+ ion irradiation, *Applied Physics Letters* **63** (20), 2803-2805 (1993).

43. K. Min, S. Kang, J. Kim, J. Yum, Y. Jhon, T. W. Hudnall, C. Bielawski, S. K. Banerjee, G. Bersuker and M. Jhon, Atomic layer etching of BeO using BCl3/Ar for the interface passivation layer of III–V MOS devices, *Microelectronic Engineering* **114**, 121-125 (2014).

44. Y. I. Jhon, K. S. Min, G. Yeom and Y. M. Jhon, Understanding time-resolved processes in atomic-layer etching of ultra-thin Al2O3 film using BCl3 and Ar neutral beam, *Applied Physics Letters* **105** (9), 093104 (2014).

45. K. Min, S. Kang, J. Kim, Y. Jhon, M. Jhon and G. Yeom, Atomic layer etching of Al2O3 using BCl3/Ar for the interface passivation layer of III–V MOS devices, *Microelectronic Engineering* **110**, 457-460 (2013).

46. J. B. Park, W. S. Lim, B. J. Park, I. H. Park, Y. W. Kim and G. Y. Yeom, Atomic layer etching of ultra-thin HfO2 film for gate oxide in MOSFET devices, *Journal of Physics D: Applied Physics* **42** (5), 055202 (2009).

47. S. Park, W. Lim, B. Park, H. Lee, J. Bae and G. Yeom, Precise depth control and low-damage atomic-layer etching of HfO2 using BCl3 and Ar neutral beam, *Electrochemical and Solid-State Letters* **11** (4), H71-H73 (2008).

48. S. Park, C. Oh, D. Lee and G. Yeom, Surface roughness variation during Si atomic layer etching by chlorine adsorption followed by an Ar neutral beam irradiation, *Electrochemical and Solid-State Letters* **8** (11), C177-C179 (2005).

49. S. Park, D. Lee and G. Yeom, Atomic layer etching of Si (100) and Si (111) using Cl2 and Ar neutral beam, *Electrochemical and Solid-State Letters* **8** (8), C106-C109 (2005).

50. S. Imai, T. Haga, O. Matsuzaki, T. Hattori and M. Matsumura, Atomic layer etching of silicon by thermal desorption method, *Japanese journal of applied physics* **34** (9R), 5049 (1995).

51. S. D. Athavale and D. J. Economou, Realization of atomic layer etching of silicon, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **14** (6), 3702-3705 (1996).

52. D. Metzler, R. L. Bruce, S. Engelmann, E. A. Joseph and G. S. Oehrlein, Fluorocarbon assisted atomic layer etching of SiO2 using cyclic Ar/C4F8 plasma, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **32** (2), 020603 (2014).

53. S. Rauf, T. Sparks, P. Ventzek, V. Smirnov, A. Stengach, K. Gaynullin and V. Pavlovsky, A molecular dynamics investigation of fluorocarbon based layer-by-layer etching of silicon and Si O 2, *Journal of Applied Physics* **101** (3), 033308 (2007).

54. N. Posseme, O. Pollet and S. Barnola, Alternative process for thin layer etching: Application to nitride spacer etching stopping on silicon germanium, *Applied Physics Letters* **105** (5), 051605 (2014).

55. J. W. Butterbaugh and A. J. Muscat, Gas phase wafer cleaning technology, *Handbook of Silicon Wafer Cleaning Technology* **2**, 269 (2008).

56. T.-W. Kim, D.-H. Kim, S.-D. Park, S. H. Shin, S. J. Jo, H.-J. Song, Y. M. Park, J.-O. Bae, Y.-W. Kim and G.-Y. Yeom, A Two-Step-Recess Process Based on Atomic-Layer Etching for High-Performance $\hbox {In} _ {0.52}\hbox {Al} _ {0.48}\hbox {As}\hbox {/}\hbox {In} _ {0.53}\hbox {Ga} _ {0.47}\hbox {As} $ p-HEMTs, *IEEE Transactions on Electron Devices* **55** (7), 1577-1584 (2008).

57. G. Y. Yeomú, Etch characteristics of TiO2 etched by using an atomic layer etching technique with BCl3 gas and an Ar neutral beam, *Journal of the Korean Physical Society* **54** (3) (2009).

58. T.-W. Kim, D.-H. Kim, S.-D. Park, S. H. Shin, S. J. Jo, H.-J. Song, Y. M. Park, J.-O. Bae, Y.-W. Kim and G.-Y. Yeom, A two-step-recess process based on atomic-layer etching for high-performance In0. 52Al0. 48As/In0. 53Ga0. 47As p-HEMTs, *IEEE Transactions on Electron Devices* **55** (7), 1577 (2008).

59. A. Alian, C. Merckling, G. Brammertz, M. Meuris, M. Heyns and K. De Meyer, InGaAs MOS transistors fabricated through a digital-etch gate-recess process and the influence of forming gas anneal on their electrical behavior, *ECS Journal of Solid State Science and Technology* **1** (6), P310-P314 (2012).

60. K. Ko and S. Pang, Controllable layer-by-layer etching of III–V compound semiconductors with an electron cyclotron resonance source, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **11** (6), 2275-2279 (1993).

61. K. Ikeda, S. Imai and M. Matsumura, Atomic layer etching of germanium, *Applied Surface Science* **112**, 87-91 (1997).

62. G. Oehrlein, D. Metzler and C. Li, Atomic layer etching at the tipping point: an overview, *ECS Journal of Solid State Science and Technology* **4** (6), N5041-N5053 (2015).

63. C. Bencher, Y. Chen, H. Dai, W. Montgomery and L. Huli, presented at the Optical Microlithography XXI, 2008 (unpublished).

64. W. Shiu, H. J. Liu, J. S. Wu, T.-L. Tseng, C. Te Liao, C. M. Liao, J. Liu and T. Wang, presented at the Optical Microlithography XXII, 2009 (unpublished).

65. F. S. Bates and G. H. Fredrickson, Block copolymer thermodynamics: theory and experiment, *Annual Review of Physical Chemistry* **41** (1), 525-557 (1990).

66. Y. Dong and R. Victora, Micromagnetic specification for bit patterned recording at 4 Tbit/in $^{2} $, *IEEE Transactions on Magnetics* **47** (10), 2652-2655 (2011).

67. S. Xiao, X. Yang, K. Y. Lee, R. J. Ver der Veerdonk, D. Kuo and T. P. Russell, Aligned nanowires and nanodots by directed block copolymer assembly, *Nanotechnology* **22** (30), 305302 (2011).

68. D. B. Millward, G. S. Lugani, R. Khurana, S. L. Light, A. Niroomand, P. D. Hustad, P. Trefonas, S.-w. Chang, C. N. Lee and D. Quach, presented at the Advanced Etch Technology for Nanopatterning III, 2014 (unpublished).

69. J. Y. Cheng, C. T. Rettner, D. P. Sanders, H. C. Kim and W. D. Hinsberg, Dense self-assembly on sparse chemical patterns: Rectifying and multiplying lithographic patterns using block copolymers, *Advanced Materials* **20** (16), 3155-3158 (2008).

70. J. Y. Cheng, D. P. Sanders, H. D. Truong, S. Harrer, A. Friz, S. Holmes, M. Colburn and W. D. Hinsberg, Simple and versatile methods to integrate directed self-assembly with optical lithography using a polarity-switched photoresist, *ACS nano* **4** (8), 4815-4823 (2010).

71. R. Ruiz, E. Dobisz and T. R. Albrecht, Rectangular patterns using block copolymer directed assembly for high bit aspect ratio patterned media, *Acs Nano* **5** (1), 79-84 (2010).

72. C.-C. Liu, E. Han, M. S. Onses, C. J. Thode, S. Ji, P. Gopalan and P. F. Nealey, Fabrication of lithographically defined chemically patterned polymer brushes and mats, *Macromolecules* **44** (7), 1876-1885 (2011).

73. G. S. Doerk, J. Y. Cheng, C. T. Rettner, S. Balakrishnan, N. Arellano and D. P. Sanders, presented at the Alternative Lithographic Technologies V, 2013 (unpublished).

74. S. Anastasiadis, T. Russell, S. Satija and C. Majkrzak, Neutron reflectivity studies of the surface-induced ordering of diblock copolymer films, *Physical Review Letters* **62** (16), 1852 (1989).

75. H. Yaegashi, K. Oyama, A. Hara, S. Natori and S. Yamauchi, presented at the Advances in Resist Materials and Processing Technology XXIX, 2012 (unpublished).

76. K. Nojiri, *Dry etching technology for semiconductors*. (Springer, 2015).

77. J. W. DuMont, A. E. Marquardt, A. M. Cano and S. M. George, Thermal Atomic Layer Etching of SiO2 by a "Conversion-Etch" Mechanism Using Sequential Reactions of Trimethylaluminum and Hydrogen Fluoride, *ACS applied materials & interfaces* **9** (11), 10296-10307 (2017).

78. H. Tompkins and E. A. Irene, *Handbook of ellipsometry*. (William Andrew, 2005).

79. C. Herzinger, B. Johs, W. McGahan, J. A. Woollam and W. Paulson, Ellipsometric determination of optical constants for silicon and thermally grown silicon dioxide via a multi-sample, multi-wavelength, multi-angle investigation, *Journal of Applied Physics* **83** (6), 3323-3336 (1998).

80. G. Jellison, Use of the biased estimator in the interpretation of spectroscopic ellipsometry data, *Applied Optics* **30** (23), 3354-3360 (1991).

81. H. G. Tompkins and W. A. McGahan, (New York: John Wiley and Sons, Inc).

82. H. Tang, F. Levy, H. Berger and P. Schmid, Urbach tail of anatase TiO 2, *Physical Review B* **52** (11), 7771 (1995).

83. A. Amtout and R. Leonelli, Optical properties of rutile near its fundamental band gap, *Physical Review B* **51** (11), 6842 (1995).

84. S.-D. Mo and W. Ching, Electronic and optical properties of three phases of titanium dioxide: Rutile, anatase, and brookite, *Physical Review B* **51** (19), 13023 (1995).

85. G. Jellison Jr and F. Modine, Parameterization of the optical functions of amorphous materials in the interband region, *Applied Physics Letters* **69** (3), 371-373 (1996).

86. Y. J. Cho, N. V. Nguyen, C. A. Richter, J. R. Ehrstein, B. H. Lee and J. C. Lee, Spectroscopic ellipsometry characterization of high-k dielectric HfO 2 thin films and the high-temperature annealing effects on their optical properties, *Applied Physics Letters* **80** (7), 1249-1251 (2002).

87. O. Buiu, Y. Lu, I. Mitrovic, S. Hall, P. Chalker and R. Potter, Spectroellipsometric assessment of HfO2 thin films, *Thin Solid Films* **515** (2), 623-626 (2006).

88. Z.-G. Ye, *Handbook of advanced dielectric, piezoelectric and ferroelectric materials: Synthesis, properties and applications*. (Elsevier, 2008).

89. D. Staaks, X. Yang, K. Y. Lee, S. D. Dhuey, S. Sassolini, I. W. Rangelow and D. L. Olynick, Low temperature dry etching of chromium towards control at sub-5 nm dimensions, *Nanotechnology* **27** (41), 415302 (2016).

90. P. Benoit-Cattin and L. C. Bernard, Anomalies of the Energy of Positive Ions Extracted from High-Frequency Ion Sources. A Theoretical Study, *Journal of Applied Physics* **39** (12), 5723-5726 (1968).

91. T. Dow and R. Scattergood, presented at the Proceedings of the ASPE winter topical meeting, 2003 (unpublished).

92. S. Chakraborty, *Mechanics over micro and nano scales*. (Springer, 2011).

93. I. Fassi and D. Shipley, *Micro-manufacturing technologies and their applications*. (Springer, 2017).

94. S. Lee, B. Park, J. S. Kim and T.-i. Kim, Designs and processes toward high-aspect-ratio nanostructures at the deep nanoscale: unconventional nanolithography and its applications, *Nanotechnology* **27** (47), 474001 (2016).

95. X. Liu, M. Wu, X. Jin, R. Chuai and J.-H. Lee, Simulation study on deep nanoscale short channel junctionless SOI FinFETs with triple-gate or double-gate structures, *Journal of Computational Electronics* **13** (2), 509-514 (2014).

96. W. I. Park, J. M. Kim, J. W. Jeong and Y. S. Jung, Deep-nanoscale pattern engineering by immersion-induced self-assembly, *ACS nano* **8** (10), 10009-10018 (2014).

97. M. Roukes, Plenty of room, indeed, *Scientific American* **285** (3), 42-49 (2001).

98. S. D. Solares, Characterization of deep nanoscale surface trenches with AFM using thin carbon nanotube probes in amplitude-modulation and frequency-force-modulation modes, *Measurement Science and Technology* **19** (1), 015503 (2007).

99. M. Perego, Focus on Sub-10nm Nanofabrication, https://iopscience.iop.org/journal/0957-4484/page/Focus-Sub-10nm-Nanofabrication, (2017).

100. T. Lill, S. Tan, K. J. Kanarik, Y. Kimura, G. Kamarthy, M. Shen, V. Vahedi, J. Marks and R. A. Gottscho, presented at the Advanced Etch Technology for Nanopatterning IV, 2015 (unpublished).

101. N. R. Council, *The new global ecosystem in advanced computing: Implications for US competitiveness and national security*. (National Academies Press, 2012).

102. K. Rupp and S. Selberherr, The economic limit to Moore's law, *IEEE Transactions on Semiconductor Manufacturing* **24** (1), 1-4 (2010).

103. K. Rupp, M. Horovitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten, Years of microprocessor trend data, *Figure available on webpage http://www.karlrupp.net/wp-content/uploads/2015* **6**.

104. S. Naffziger, presented at the 2006 Symposium on VLSI Circuits, 2006. Digest of Technical Papers., 2006 (unpublished).

105. G. E. Moore, (McGraw-Hill New York, NY, USA:, 1965).

106. G. E. Moore, Cramming more components onto integrated circuits, *Proceedings of the IEEE* **86** (1), 82-85 (1998).

107. Y. Shiroishi, K. Fukuda, I. Tagawa, H. Iwasaki, S. Takenoiri, H. Tanaka, H. Mutoh and N. Yoshikawa, Future options for HDD storage, *IEEE Transactions on Magnetics* **45** (10), 3816-3822 (2009).

108. M. J. Madou, *Fundamentals of microfabrication: the science of miniaturization*. (CRC press, 2002).

109. R. C. O'Handley, Model for strain and magnetization in magnetic shape-memory alloys, *Journal of Applied Physics* **83** (6), 3263-3270 (1998).

110. O. Hellwig, E. E. Marinero and D. K. Weller, (Google Patents, 2012).

111. O. Hellwig, E. E. Marinero, D. Kercher, T. Hennen, A. McCallum, E. Dobisz, T.-W. Wu, J. Lille, T. Hirano and R. Ruiz, Bit patterned media optimization at 1 Tdot/in2 by post-annealing, *Journal of Applied Physics* **116** (12), 123913 (2014).

112. A. Keshavarzi, A. T. Haghighat and M. Bohlouli, presented at the Intelligent Data Acquisition and Advanced Computing Systems (IDAACS), 2013 IEEE 7th International Conference on, 2013 (unpublished).

113. R. H. Zakon, Hobbes' Internet Timeline 25, https://www.zakon.org/robert/internet/timeline/, (2010).

114. A. Moser, K. Takano, D. T. Margulies, M. Albrecht, Y. Sonobe, Y. Ikeda, S. Sun and E. E. Fullerton, Magnetic recording: advancing into the future, *Journal of Physics D: Applied Physics* **35** (19), R157 (2002).

115. I. Research, History Highlights, History of IBM Research 1945–1998, http://www.research.ibm.com/about/past_history.shtml, (2010).

116. R. New, The future of magnetic recording technology, *Hitachi Global Storage Technologies* (2008).

117. ASTC, ASTC Technology Roadmap, http://idema.org/wp-content/plugins/download-monitor/download.php?id=2456, (2016).

118. R. Sbiaa and S. N. Piramanayagam, Patterned media towards nano-bit magnetic recording: Fabrication and challenges, *Recent patents on nanotechnology* **1** (1), 29-40 (2007).

119. A. Kikitsu, Y. Kamata, M. Sakurai and K. Naito, Recent progress of patterned media, *IEEE Transactions on Magnetics* **43** (9), 3685-3688 (2007).

120. C. Ross, Magnetic Recording: Patterned Media, (2001).

121. B. Lu, D. Weller and G. Ju, (Google Patents, 2005).

122. S. Y. Chou, M. S. Wei, P. R. Krauss and P. B. Fischer, Single-domain magnetic pillar array of 35 nm diameter and 65 Gbits/in. 2 density for ultrahigh density quantum magnetic storage, *Journal of Applied Physics* **76** (10), 6673-6675 (1994).

123. R. New, R. Pease and R. White, Submicron patterning of thin cobalt films for magnetic storage, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **12** (6), 3196-3201 (1994).

124. T. R. Albrecht, O. Hellwing, R. Ruiz, M. E. Schabes, B. D. Terris and X. Z. Wu, in *Nanoscale Magnetic Materials and Applications* (Springer, 2009), pp. 237-274.

125. S. J. Greaves, Y. Kanai and H. Muraoka, Magnetic recording in patterned media at 5–10 Tb/in $^{2} $, *IEEE Transactions on Magnetics* **44** (11), 3430-3433 (2008).

126. M. Lubarda, S. Li, B. Livshitz, E. Fullerton and V. Lomakin, Reversal in bit patterned media with vertical and lateral exchange, *IEEE Transactions on Magnetics* **47** (1), 18-25 (2010).

127. M. E. Schabes, Micromagnetic simulations for terabit/in2 head/media systems, *Journal of Magnetism and Magnetic Materials* **320** (22), 2880-2884 (2008).

128. Y. Shiroishi, K. Fukuda, I. Tagawa, H. Iwasaki, S. Takenoiri, H. Tanaka, H. Mutoh and N. Yoshikawa, Future options for HDD storage, *Magnetics, IEEE Transactions on* **45** (10), 3816-3822 (2009).

129. T. R. Albrecht and M. E. Schabes, (Google Patents, 2011).

130. J. Lille, K. Patel, R. Ruiz, T.-W. Wu, H. Gao, L. Wan, G. Zeltzer, E. Dobisz and T. Albrecht, presented at the SPIE Photomask Technology, 2011 (unpublished).

131. B. Terris, Fabrication challenges for patterned recording media, *Journal of Magnetism and Magnetic Materials* **321** (6), 512-517 (2009).

132. H. Richter, A. Dobin, R. Lynch, D. Weller, R. Brockie, O. Heinonen, K. Gao, J. Xue, R. vd Veerdonk and P. Asselin, Recording potential of bit-patterned media, *Applied physics letters* **88** (22), 222512 (2006).

133. S. Dallorto, D. Staaks, A. Schwartzberg, X. Yang, K. Y. Lee, I. W. Rangelow, S. Cabrini and D. L. Olynick, Atomic layer deposition for spacer defined double patterning of sub-10 nm titanium dioxide features, *Nanotechnology* **29** (40), 405302 (2018).

134. T. R. Albrecht, H. Arora, V. Ayanoor-Vitikkate, J.-M. Beaujour, D. Bedau, D. Berman, A. L. Bogdanov, Y.-A. Chapuis, J. Cushen and E. E. Dobisz, Bit-patterned magnetic recording: Theory, media fabrication, and recording performance, *IEEE Transactions on Magnetics* **51** (5), 1-42 (2015).

135. X. Yang, L. Wan, S. Xiao, Y. Xu and D. K. Weller, Directed block copolymer assembly versus electron beam lithography for bit-patterned media with areal density of 1 terabit/inch2 and beyond, *ACS nano* **3** (7), 1844-1858 (2009).

136. S. Y. Chou, Patterned magnetic nanostructures and quantized magnetic disks, *Proceedings of the IEEE* **85** (4), 652-671 (1997).

137. D. A. Thompson and J. S. Best, The future of magnetic data storage techology, *IBM Journal of Research and Development* **44** (3), 311-322 (2000).

138. X. Yang, S. Xiao, W. Wu, Y. Xu, K. Mountfield, R. Rottmayer, K. Lee, D. Kuo and D. Weller, Challenges in 1 Teradot/ in. 2 dot patterning using electron beam lithography for bit-patterned media, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **25** (6), 2202-2209 (2007).

139. S. Okazaki, Resolution limits of optical lithography, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **9** (6), 2829-2833 (1991).

140. V. R. Manfrinato, L. Zhang, D. Su, H. Duan, R. G. Hobbs, E. A. Stach and K. K. Berggren, Resolution limits of electron-beam lithography toward the atomic scale, *Nano Letters* **13** (4), 1555-1558 (2013).

141. E. A. Dobisz, Z. Z. Bandic, T.-W. Wu and T. Albrecht, Patterned media: nanofabrication challenges of future disk drives, *Proceedings of the IEEE* **96** (11), 1836-1846 (2008).

142. M. D. Austin, H. Ge, W. Wu, M. Li, Z. Yu, D. Wasserman, S. Lyon and S. Y. Chou, Fabrication of 5 nm linewidth and 14 nm pitch features by nanoimprint lithography, *Applied Physics Letters* **84** (26), 5299-5301 (2004).

143. C. Peroz, S. Dhuey, M. Cornet, M. Vogler, D. Olynick and S. Cabrini, Single digit nanofabrication by step-and-repeat nanoimprint lithography, *Nanotechnology* **23** (1), 015305 (2011).

144. S. Owa, H. Nagasaka, K. Nakano and Y. Ohmura, presented at the SPIE 31st International Symposium on Advanced Lithography, 2006 (unpublished).

145. Y. Borodovsky, presented at the SPIE 31st International Symposium on Advanced Lithography, 2006 (unpublished).

146. A. Raley, S. Thibaut, N. Mohanty, K. Subhadeep, S. Nakamura, A. Ko, D. O'Meara, K. Tapily, S. Consiglio and P. Biolsi, A spacer-on-spacer scheme for self-aligned multiple patterning and integration.

147. Z. Yu, W. Wu, L. Chen and S. Y. Chou, Fabrication of large area 100 nm pitch grating by spatial frequency doubling and nanoimprint lithography for subwavelength optical applications, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **19** (6), 2816-2819 (2001).

148. S. Dhuey, C. Peroz, D. Olynick, G. Calafiore and S. Cabrini, Obtaining nanoimprint template gratings with 10 nm half-pitch by atomic layer deposition enabled spacer double patterning, *Nanotechnology* **24** (10), 105303 (2013).

149. J. Beynet, P. Wong, A. Miller, S. Locorotondo, D. Vangoidsenhoven, T.-H. Yoon, M. Demand, H.-S. Park, T. Vandeweyer, H. Sprey, Y.-M. Yoo and M. Maenhoudt, presented at the SPIE Lithography Asia, 2009 (unpublished).

150. H. Profijt, S. Potts, M. Van de Sanden and W. Kessels, Plasma-assisted atomic layer deposition: basics, opportunities, and challenges, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **29** (5), 050801 (2011).

151. J. Beynet, P. Wong, A. Miller, S. Locorotondo, D. Vangoidsenhoven, T.-H. Yoon, M. Demand, H.-S. Park, T. Vandeweyer and H. Sprey, presented at the Lithography Asia 2009, 2009 (unpublished).

152. C. H. Bak, S. J. Ku, G. C. Jo, K. Jung, H. J. Lee, S. H. Kwon and J.-B. Kim, Ultrahigh density sub-10 nm TiO2 nanosheet arrays with high aspect ratios via the spacer-defined double-patterning process, *Polymer* **60**, 267-273 (2015).

153. A. Mackus, A. Bol and W. Kessels, The use of atomic layer deposition in advanced nanopatterning, *Nanoscale* **6** (19), 10941-10960 (2014).

154. H. S. Moon, J. Y. Kim, H. M. Jin, W. J. Lee, H. J. Choi, J. H. Mun, Y. J. Choi, S. K. Cha, S. H. Kwon and S. O. Kim, Atomic layer deposition assisted pattern multiplication of block copolymer lithography for 5 nm scale nanopatterning, *Advanced Functional Materials* **24** (27), 4343-4348 (2014).

155. R. A. Gottscho, C. W. Jurgensen and D. Vitkavage, Microscopic uniformity in plasma etching, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **10** (5), 2133-2147 (1992).

156. R. A. Griffiths, A. Williams, C. Oakland, J. Roberts, A. Vijayaraghavan and T. Thomson, Directed self-assembly of block copolymers for use in bit patterned media fabrication, *Journal of Physics D: Applied Physics* **46** (50), 503001 (2013).

157. K. Patel, R. Ruiz, J. Lille, L. Wan, E. Dobiz, H. Gao, N. Robertson and T. Albrecht, Line-frequency doubling of directed self-assembly patterns for single-digit bit pattern media lithography, *Pro. SPIE* **8323**, 83230U (2012).

158. Z. Liu, Y. Wu, B. Harteneck and D. Olynick, Super-selective cryogenic etching for sub-10 nm features, *Nanotechnology* **24** (1), 015305 (2012).

159. D. L. Olynick, J. A. Liddle and I. W. Rangelow, Profile evolution of Cr masked features undergoing HBr-inductively coupled plasma etching for use in 25 nm silicon nanoimprint templates, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **23** (5), 2073-2077 (2005).

160. C. C. Welch, D. L. Olynick, Z. Liu, A. Holmberg, C. Peroz, A. P. Robinson, M. D. Henry, A. Scherer, T. Mollenhauer and V. Genova, presented at the International Conference on Micro-and Nano-Electronics 2012, 2013 (unpublished).

161. X. Gu, Z. Liu, I. Gunkel, S. Chourou, S. W. Hong, D. L. Olynick and T. P. Russell, High Aspect Ratio Sub-15 nm Silicon Trenches From Block Copolymer Templates, *Advanced Materials* **24** (42), 5688-5694 (2012).

162. J. Van Hemmen, S. Heil, J. Klootwijk, F. Roozeboom, C. Hodson, M. Van de Sanden and W. Kessels, Plasma and thermal ALD of Al2O3 in a commercial 200 mm ALD reactor, *Journal of the Electrochemical Society* **154** (7), G165-G169 (2007).

163. Q. Peng, Y. C. Tseng, S. B. Darling and J. W. Elam, Nanoscopic patterned materials with tunable dimensions via atomic layer deposition on block copolymers, *Advanced Materials* **22** (45), 5129-5133 (2010).

164. Y.-C. Tseng, Q. Peng, L. E. Ocola, D. A. Czaplewski, J. W. Elam and S. B. Darling, Etch properties of resists modified by sequential infiltration synthesis, *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **29** (6), 06FG01 (2011).

165. R. Ruiz, L. Wan, J. Lille, K. C. Patel, E. Dobisz, D. E. Johnston, K. Kisslinger and C. T. Black, Image quality and pattern transfer in directed self assembly with block-selective atomic layer deposition, *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **30** (6), 06F202 (2012).

166. Y.-C. Tseng, Q. Peng, L. E. Ocola, D. A. Czaplewski, J. W. Elam and S. B. Darling, Enhanced polymeric lithography resists via sequential infiltration synthesis, *Journal of Materials Chemistry* **21** (32), 11722-11725 (2011).

167. Y.-C. Tseng, Q. Peng, L. E. Ocola, J. W. Elam and S. B. Darling, Enhanced block copolymer lithography using sequential infiltration synthesis, *The Journal of Physical Chemistry C* **115** (36), 17725-17729 (2011).

168. M. Ramanathan, Y.-C. Tseng, K. Ariga and S. B. Darling, Emerging trends in metal-containing block copolymers: synthesis, self-assembly, and nanomanufacturing applications, *Journal of Materials Chemistry C* **1** (11), 2080-2091 (2013).

169. Y.-H. Ting, S.-M. Park, C.-C. Liu, X. Liu, F. Himpsel, P. F. Nealey and A. E. Wendt, Plasma etch removal of poly (methyl methacrylate) in block copolymer lithography, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **26** (5), 1684-1689 (2008).

170. Q. Peng, Y.-C. Tseng, S. B. Darling and J. W. Elam, A route to nanoscopic materials via sequential infiltration synthesis on block copolymer templates, *Acs Nano* **5** (6), 4600-4606 (2011).

171. B. Burton, S. Kang, S. Rhee and S. George, SiO2 atomic layer deposition using tris (dimethylamino) silane and hydrogen peroxide studied by in situ transmission FTIR spectroscopy, *The Journal of Physical Chemistry C* **113** (19), 8249-8257 (2009).

172. B. Abendroth, T. Moebus, S. Rentrop, R. Strohmeyer, M. Vinnichenko, T. Weling, H. Stöcker and D. C. Meyer, Atomic layer deposition of TiO 2 from tetrakis (dimethylamino) titanium and H 2 O, *Thin Solid Films* **545**, 176-182 (2013).

173. D. Mitchell, G. Triani, D. Attard, K. Finnie, P. Evans, C. Barbé and J. Bartlett, Atomic layer deposition of TiO2 and Al2O3 thin films and nanolaminates, *Smart Materials and Structures* **15** (1), S57 (2005).

174. M. A. Lieberman and A. J. Lichtenberg, Principles of plasma discharges and materials processing, *MRS Bulletin* **30** (12), 899-901 (1994).

175. C. Steinbrüchel, Universal energy dependence of physical and ion-enhanced chemical etch yields at low ion energy, *Applied Physics Letters* **55** (19), 1960-1962 (1989).

176. M. R. Baklanov, J.-F. de Marneffe, D. Shamiryan, A. M. Urbanowicz, H. Shi, T. V. Rakhimova, H. Huang and P. S. Ho, Plasma processing of low-k dielectrics, *Journal of Applied Physics* **113** (4), 4 (2013).

177. J. Hopwood, Review of inductively coupled plasmas for plasma processing, *Plasma Sources Science and Technology* **1** (2), 109 (1992).

178. A. Popov Oleg, (Noyes publication, Park Ridge, New Jersey, 1995).

179. M. A. Lieberman and A. J. Lichtenberg, *Principles of plasma discharges and materials processing*. (John Wiley & Sons, 2005).

180. M. D. Henry, California Institute of Technology, 2010.

181. D. L. Flamm, V. M. Donnelly and J. A. Mucha, The reaction of fluorine atoms with silicon, *Journal of Applied Physics* **52** (5), 3633-3639 (1981).

182. V. M. Donnelly, D. L. Flamm, W. Dautremont-Smith and D. Werder, Anisotropic etching of SiO2 in low-frequency CF4/O2 and NF3/Ar plasmas, *Journal of Applied Physics* **55** (1), 242-252 (1984).

183. J. Coburn, I nsitu Auger electron spectroscopy of Si and SiO2 surfaces plasma etched in CF4-H2 glow discharges, *Journal of Applied Physics* **50** (8), 5210-5213 (1979).

184. C. Li, D. Metzler, C. S. Lai, E. A. Hudson and G. S. Oehrlein, Fluorocarbon based atomic layer etching of Si3N4 and etching selectivity of SiO2 over Si3N4, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **34** (4), 041307 (2016).

185. T. Standaert, C. Hedlund, E. Joseph, G. Oehrlein and T. Dalton, Role of fluorocarbon film formation in the etching of silicon, silicon dioxide, silicon nitride, and amorphous hydrogenated silicon carbide, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **22** (1), 53-60 (2004).

186. G. S. Oehrlein, Surface processes in low pressure plasmas, *Surface Science* **386** (1-3), 222-230 (1997).

187. M. Schaepkens and G. S. Oehrlein, A review of SiO2 etching studies in inductively coupled fluorocarbon plasmas, *Journal of the Electrochemical Society* **148** (3), C211-C221 (2001).

188. A. Sankaran and M. J. Kushner, Fluorocarbon plasma etching and profile evolution of porous low-dielectric-constant silica, *Applied Physics Letters* **82** (12), 1824-1826 (2003).

189. J. Matsui, N. Nakano, Z. L. Petrović and T. Makabe, The effect of topographical local charging on the etching of deep-submicron structures in SiO 2 as a function of aspect ratio, *Applied Physics Letters* **78** (7), 883-885 (2001).

190. K. P. Giapis and G. S. Hwang, Pattern-dependent charging and the role of electron tunneling, *Japanese journal of applied physics* **37** (4S), 2281 (1998).

191. G. S. Hwang and K. P. Giapis, On the origin of the notching effect during etching in uniform high density plasmas, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **15** (1), 70-87 (1997).

192. T. Kamata and H. Arimoto, Charge build-up in Si-processing plasma caused by electron shading effect, *Journal of Applied Physics* **80** (5), 2637-2642 (1996).

193. S. Ogino, N. Fujiwara, H. Miyatake and M. Yoneda, Influence of poly-Si potential on profile distortion caused by charge accumulation, *Japanese journal of applied physics* **35** (4S), 2445 (1996).

194. K. Hashimoto, New phenomena of charge damage in plasma etching: Heavy damage only through dense-line antenna, *Japanese journal of applied physics* **32** (12S), 6109 (1993).

195. O. Joubert, P. Czuprynski, F. Bell, P. Berruyer and R. Blanc, Analyses of the chemical topography of silicon dioxide contact holes etched in a high density plasma source, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **15** (3), 629-639 (1997).

196. M. Wang and M. J. Kushner, High energy electron fluxes in dc-augmented capacitively coupled plasmas. II. Effects on twisting in high aspect ratio etching of dielectrics, *Journal of Applied Physics* **107** (2), 023309 (2010).

197. P. Garrou, C. Bower and P. Ramm, *Handbook of 3D Integration, Volume 1: Technology and Applications of 3D Integrated Circuits*. (John Wiley & Sons, 2011).

198. J. P. Chang, J. C. Arnold, G. C. Zau, H.-S. Shin and H. H. Sawin, Kinetic study of low energy argon ion-enhanced plasma etching of polysilicon with atomic/molecular chlorine, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **15** (4), 1853-1863 (1997).

199. H. Shin, W. Zhu, L. Xu, V. M. Donnelly and D. J. Economou, Control of ion energy distributions using a pulsed plasma with synchronous bias on a boundary electrode, *Plasma Sources Science and Technology* **20** (5), 055001 (2011).

200. L. Xu, D. J. Economou, V. M. Donnelly and P. Ruchhoeft, Extraction of a nearly monoenergetic ion beam using a pulsed plasma, *Applied Physics Letters* **87** (4), 041502 (2005).

201. H. Shin, W. Zhu, V. M. Donnelly and D. J. Economou, Surprising importance of photo-assisted etching of silicon in chlorine-containing plasmas, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **30** (2), 021306 (2012).

202. K. J. Kanarik, S. Tan, W. Yang, T. Kim, T. Lill, A. Kabansky, E. A. Hudson, T. Ohba, K. Nojiri and J. Yu, Predicting synergy in atomic layer etching, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **35** (5), 05C302 (2017).

203. V. Smirnov, A. Stengach, K. Gaynullin, V. Pavlovsky, S. Rauf, P. Stout and P. Ventzek, Molecular-dynamics model of energetic fluorocarbon-ion bombardment on SiO 2 I. Basic model and CF 2+-ion etch characterization, *Journal of Applied Physics* **97** (9), 093302 (2005).

204. D. Metzler, C. Li, S. Engelmann, R. L. Bruce, E. A. Joseph and G. S. Oehrlein, Fluorocarbon assisted atomic layer etching of SiO2 and Si using cyclic Ar/C4F8 and Ar/CHF3 plasma, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **34** (1), 01B101 (2016).

205. A. V. Vasenkov, X. Li, G. S. Oehrlein and M. J. Kushner, Properties of c-C 4 F 8 inductively coupled plasmas. II. Plasma chemistry and reaction mechanism for modeling of Ar/c-C 4 F 8/O 2 discharges, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **22** (3), 511-530 (2004).

206. A. Sankaran and M. J. Kushner, Integrated feature scale modeling of plasma processing of porous and solid SiO 2. I. Fluorocarbon etching, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **22** (4), 1242-1259 (2004).

207. D. Metzler, C. Li, S. Engelmann, R. L. Bruce, E. A. Joseph and G. S. Oehrlein, Characterizing fluorocarbon assisted atomic layer etching of Si using cyclic Ar/C4F8 and Ar/CHF3 plasma, *The Journal of chemical physics* **146** (5), 052801 (2017).

208. K. J. Kanarik, S. Tan and R. A. Gottscho, Atomic layer etching: rethinking the art of etch, *The journal of physical chemistry letters* **9** (16), 4814-4821 (2018).

209. P. D. Agnello, Process requirements for continued scaling of CMOS—the need and prospects for atomic-level manipulation, *IBM Journal of Research and Development* **46** (2.3), 317-338 (2002).

210. A. D. Bailey III and R. A. Gottscho, Aspect ratio independent etching: Fact or fantasy?, *Japanese journal of applied physics* **34** (4S), 2083 (1995).

211. T. Faraz, F. Roozeboom, H. Knoops and W. Kessels, Atomic layer etching: what can we learn from atomic layer deposition?, *ECS Journal of Solid State Science and Technology* **4** (6), N5023-N5032 (2015).

212. S. D. Athavale and D. J. Economou, Molecular dynamics simulation of atomic layer etching of silicon, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **13** (3), 966-971 (1995).

213. S. W. King, Dielectric barrier, etch stop, and metal capping materials for state of the art and beyond metal interconnects, *ECS Journal of Solid State Science and Technology* **4** (1), N3029-N3047 (2015).

214. M. Schaepkens, T. Standaert, N. Rueger, P. Sebel, G. Oehrlein and J. Cook, Study of the SiO 2-to-Si 3 N 4 etch selectivity mechanism in inductively coupled fluorocarbon plasmas and a comparison with the SiO 2-to-Si mechanism, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **17** (1), 26-37 (1999).

215. D. C. Marra and E. S. Aydil, Effect of H 2 addition on surface reactions during CF 4/H 2 plasma etching of silicon and silicon dioxide films, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **15** (5), 2508-2517 (1997).

216. K. J. Kanarik, S. Tan, J. Holland, A. Eppler, V. Vahedi, J. Marks and R. A. Gottscho, Moving atomic layer etch from lab to tab, *Solid State Technology* **56** (8), 14-17 (2013).

217. D. Gahan, S. Daniels, C. Hayden, D. O'Sullivan and M. Hopkins, Characterization of an asymmetric parallel plate radio-frequency discharge using a retarding field energy analyzer, *Plasma Sources Science and Technology* **21** (1), 015002 (2011).

218. D. Gahan, B. Dolinaj and M. Hopkins, Retarding field analyzer for ion energy distribution measurements at a radio-frequency biased electrode, *Review of Scientific Instruments* **79** (3), 033502 (2008).

219. R. Gottscho and K. Kanarik, APS 64th Annual GEC, *Salt Lake City, UT* (2011).

220. T.-C. Wei and C.-H. Liu, Evaluation of plasma deposited fluorocarbon films using experimental design methodology, *Surface and Coatings Technology* **200** (7), 2214-2222 (2005).

221. D. Flamm, C. Mogab and E. Sklaver, Reaction of fluorine atoms with SiO2, *Journal of Applied Physics* **50** (10), 6211-6213 (1979).

222. S. Tachi, K. Tsujimoto and S. Okudaira, Low-temperature reactive ion etching and microwave plasma etching of silicon, *Applied Physics Letters* **52** (8), 616-618 (1988).

223. C. M. Huard, S. Sriraman, A. Paterson and M. J. Kushner, Transient behavior in quasi-atomic layer etching of silicon dioxide and silicon nitride in fluorocarbon plasmas, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **36** (6), 06B101 (2018).

224. R. J. Gasvoda, A. W. van de Steeg, R. Bhowmick, E. A. Hudson and S. Agarwal, Surface phenomena during plasma-assisted atomic layer etching of SiO2, *ACS applied materials & interfaces* **9** (36), 31067-31075 (2017).

225. K. J. Kanarik, G. Kamarthy and R. A. Gottscho, Plasma etch challenges for FinFET transistors, *Solid State Technology* **55** (3), 15-17 (2012).

226. S. Dallorto, A. Goodyear, M. Cooke, J. E. Szornel, C. Ward, C. Kastl, A. Schwartzberg, I. W. Rangelow and S. Cabrini, Atomic layer etching of SiO2 with Ar and CHF 3 plasmas: A self-limiting process for aspect ratio independent etching, *Plasma Processes and Polymers*, e1900051.

227. D. Metzler, K. Uppireddi, R. L. Bruce, H. Miyazoe, Y. Zhu, W. Price, E. S. Sikorski, C. Li, S. U. Engelmann and E. A. Joseph, Application of cyclic fluorocarbon/argon discharges to device patterning, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **34** (1), 01B102 (2016).

228. K. H. Kirmse, A. E. Wendt, G. S. Oehrlein and Y. Zhang, Fluorocarbon high density plasmas. VIII. Study of the ion flux composition at the substrate in electron cyclotron resonance etching processes using fluorocarbon gases, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **12** (4), 1287-1292 (1994).

229. J. Butterbaugh, D. Gray and H. Sawin, Plasma–surface interactions in fluorocarbon etching of silicon dioxide, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **9** (3), 1461-1470 (1991).

230. R. Seeböck, W. Köhler and M. Römheld, Pressure dependence of the mean electron energy in the bulk plasma of an rf discharge in argon, *Contributions to Plasma Physics* **32** (6), 613-622 (1992).

231. K. Maruyama, K. Ohkouchi, Y. Ohtsu and T. Goto, CF3, CF2 and CF radical measurements in RF CHF3 etching plasma using infrared diode laser absorption spectroscopy, *Japanese journal of applied physics* **33** (7S), 4298 (1994).

232. D. Q. Wen, Y. R. Zhang, M. A. Lieberman and Y. N. Wang, Ion Energy and Angular Distribution in Biased Inductively Coupled Ar/O2 Discharges by Using a Hybrid Model, *Plasma Processes and Polymers* **14** (4-5), 1600100 (2017).

233. K. Takahashi and K. Ono, Selective etching of high-k Hf O 2 films over Si in hydrogen-added fluorocarbon (CF 4/ Ar/ H 2 and C 4 F 8/ Ar/ H 2) plasmas, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **24** (3), 437-443 (2006).

234. M. Fukasawa, Y. Nakakubo, A. Matsuda, Y. Takao, K. Eriguchi, K. Ono, M. Minami, F. Uesawa and T. Tatsumi, Structural and electrical characterization of HBr/O2 plasma damage to Si substrate, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **29** (4), 041301 (2011).

235. N. Kuboi, T. Tatsumi, T. Kinoshita, T. Shigetoshi, M. Fukasawa, J. Komachi and H. Ansai, Prediction of plasma-induced damage distribution during silicon nitride etching using advanced three-dimensional voxel model, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **33** (6), 061308 (2015).

236. A. M. Mohs, M. C. Mancini, S. Singhal, J. M. Provenzale, B. Leyland-Jones, M. D. Wang and S. Nie, Hand-held spectroscopic device for in vivo and intraoperative tumor detection: contrast enhancement, detection sensitivity, and tissue penetration, *Analytical Chemistry* **82** (21), 9058-9065 (2010).

237. S. Noda, N. Ozawa, T. Kinoshita, H. Tsuboi, K. Kawashima, Y. Hikosaka, K. Kinoshita and M. Sekine, Investigation of ion transportation in high-aspect-ratio holes from fluorocarbon plasma for SiO2 etching, *Thin Solid Films* **374** (2), 181-189 (2000).

238. N. Fox-Lyon, D. Metzler, G. S. Oehrlein, D. Farber and T. Lii, Controlling Asymmetric Photoresist Feature Dimensions during Plasma-Assisted Shrink, *Plasma Processes and Polymers* **11** (7), 714-720 (2014).

239. A. J. Bariya, H. Shan, C. W. Frank, S. A. Self and J. P. McVittie, The etching of CHF3 plasma polymer in fluorine-containing discharges, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **9** (1), 1-7 (1991).

240. A. J. Bariya, C. W. Frank and J. P. McVittie, A surface kinetic model for plasma polymerization with application to plasma etching, *Journal of the Electrochemical Society* **137** (8), 2575-2581 (1990).

241. K.-Y. Lin, C. Li, S. Engelmann, R. L. Bruce, E. A. Joseph, D. Metzler and G. S. Oehrlein, Achieving ultrahigh etching selectivity of SiO2 over Si3N4 and Si in atomic layer etching by exploiting chemistry of complex hydrofluorocarbon precursors, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **36** (4), 040601 (2018).

242. J. Kim, M. Rao, M. Cappelli, S. Sharma and M. Meyyappan, Mass spectrometric and Langmuir probe measurements in inductively coupled plasmas in Ar, CHF3/Ar and CHF3/Ar/O2 mixtures, *Plasma Sources Science and Technology* **10** (2), 191 (2001).

Thesis

1. Critical dimensions in manufacturing have been shrinking aggressively and today fabrication is dealing with devices requiring atomic scale precision.

2. The breakthrough for achieving control of matter at the atomic scale, can be found in atomic scale processing. Atomic layer deposition (ALD) and Atomic layer etching (ALE) are material fabrication processes which enable atomic scale control.

3. Spacer defined double patterning (SDDP) is used for line pitch scaling in sub-10 nm fabrication, relying on an increasing number of deposition and etch steps.

4. For the first time, the fabrication of 7.5 nm titanium oxide features using SDDP and ALD for spacer engineering is demonstrated.

5. The demand for controlled etching at the atomic scale with low damage is answered using ALE. An ALE process removes near atomic monolayers of materials alternating between a reaction step where a more volatile layer is created and a desorption step, where the volatile layer is removed. Using ions allows for the direction etching required to form deep narrow structures.

6. In Fluorocarbon-based ALE of SiO_2, first, a thin fluorocarbon layer is deposited using CHF_3 plasma, followed by an Ar^+ ion plasma which removes the fluorinated SiO_2 layer (mixed layer), and the fluorocarbon layer.

7. Plasma parameters, e.g. Ar^+ ion energies, pressure, deposition step length, etch step length, and substrate electrode temperature impact the etch performance. Using a conventional plasma tool, the ALE windows of SiO_2 is achieved and, consequently, self-limiting behavior is observed.

8. For the first time, using the fluorocarbon-based ALE process, aspect ratio independent etching and high fidelity pattern transferring are achieved. Nanoscale trench sizes can be etched with a sidewall angle of 87˚±1.5˚ and undercut values as low as 3.7±0.5%, which confirms previous theoretical calculations.

Publications

Published Papers

S. Hernández, V. Cauda, A. Chiodoni, Stefano Dallorto, A. Sacco, D. Hidalgo, E. Celasco, C. F. Pirri, Optimization of 1D ZnO@TiO_2 core–shell nanostructures for enhanced photoelectrochemical water splitting under solar light illumination, *ACS Appl. Mater. Interfaces* 6 (15), 12153-12167 (2014).

I. W. Rangelow, A. Ahmad, T. Ivanov, M. Kaestner, Y. Krivoshapkina, T. Angelov, S. Lenk, C. Lenk, V. Ishchuk, M. Hofmann, D. Nechepurenko, I. Atanasov, B. Volland, E. Guliyev, Z. Durrani, M. Jones, C. Wang, D. Liu, A. Reum, M. Holz, N. Nikolov, W. Majstrzyk, T. Gotszalk, D. Staaks, Stefano Dallorto, and D. L. Olynick, Pattern-generation and pattern-transfer for single-digit nano devices, *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom.* 34 (6), 06K202 (2016),

R. Mincigrucci, A. Matruglio, A. Calvi, L. Foglia, E. Principi, A. Simoncig, F. Bencivenga, Stefano Dallorto, A. Gessini and G. Kurdi, D. Olynick, S. Dhuey, R. Sergo, M. Lazzarino, C. Masciovecchio, S. Dal Zilio, Toward an integrated device for spatiotemporal superposition of free-electron lasers and laser pulses, *Optics Letters* 41 (21), 5090-5093 (2016).

Stefano Dallorto, D. Staaks, A. Schwartzberg, X. Yang, K. Y. Lee, I. W. Rangelow, S. Cabrini and D. L. Olynick, Atomic layer deposition for spacer defined double patterning of sub-10 nm titanium dioxide features, *Nanotechnology* 29 (40), 405302 (2018).

Stefano Dallorto, A. Goodyear, M. Cooke, J. E. Szornel, C. Ward, C. Kastl, A. Schwartzberg, I. W. Rangelow and S. Cabrini, Atomic layer etching of SiO_2 with Ar and CHF_3 plasmas: A self-limiting process for aspect ratio independent etching, *Plasma Processes Polym.*, e1900051.

M Hofmann, S. Mecholdt, M. Mohr, M. Holz, Stefano Dallorto, E. Manske, H. J. Fecht, I. W. Rangelow, Nanoscale Lift-Off Process Using Field Emission Scanning Probe Lithography, *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom.* (2019).

Stefano Dallorto, M. Lorenzon, J. E. Szornel, A. Schwartzberg, A. Goodyear, M. Cooke, I. W. Rangelow, S. Cabrini, Balancing Ion Parameters and FC Chemical reactants for SiO_2 Pattern Transfer Control using Fluorocarbon-Based Atomic Layer Etching, *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom.* (2019).

Manuscript to be submitted

Stefano Dallorto, M. Elowson, M. Lorenzon, M. V. Altoe, A. Goodyear, M. Cooke, I. W. Rangelow, S. Cabrini, A. Schwartzberg, S. Aloni, Surface chemistry during Fluorocarbon-based atomic layer etching of SiO_2 with CHF_3 and Ar plasmas.