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Aluminium packages for MEMS devices

MICRO- AND NANOELECTRONICS

The problems of the microelectronic packaging are well-known. Among them are a wide variety of materials, technologies, designs, standard sizes to keep the device mastering back and to block the increase in the integration scale, and the improvement of the mass-size parameters of the devices. The automation of assembling is complicated, schedule times are extended and funds to testing are wasted. At the same time it should be noted that a wide variety of package types is available: ceramic leadless chip carriers and chip carriers provided with leads, plastic packages with leads, plastic and ceramic flatpacks with leads on each of four sides, housings with the lead arrays, etc. However, a diversity of the technologies, materials and the package types are evidence of problems still remain to be solved. The heat dissipation, protection against electromagnetic radiation and frequency characteristics are among the most essential problems. It is obvious that the use of the metal packages facilitates the progress in the solution of the first of two problems. A certain experience in the use of metal (glass-to-metal) packages is gained in the hybrid technology while it is still a question the utilization of metal packages in the VLSI technology. So, the technologies and constructions of the chip-carrier packages and housings based on the anodization of the aluminum alloys we developed are of considerable interest.

We have developed two design variants of packages with flexible leads and one leadless package.

The packages with flexible leads are the most commonly used for the time being. This is conditioned mainly by their universality, namely, their ability to be mounted on the conventional printed boards as well as on other bases used in the hybrid technology. The flexible leads allow drastic reducing the demands in the matching of the thermal coefficients of the linear expansion between materials of the substrate and the package to mount the packages on anyone substrate using the modern surface mounting. An assembly framework on the substrate using a ceramic base and thick-film conductors positioned on the base to make leads from totally enclosed casing form the basis of packages with flexible leads [1]. Such the package design excludes the use of metal-glass soldered joints and sealing gaskets between the substrate and framework to improve considerably thermal characteristics of the housing. However, large size and weight of the package are the main disadvantages of the design.

The first variant of packages with flexible leads uses a planar aluminum substrate with the anodic dielectric layer and film elements on its surface. Film metallization is fabricated by the anodic alumina technology [2] including the electron-beam deposition of the aluminum films, the photolithography, and the anodization. The produced bases provide high mechanical strength, sufficient hardness of the dielectric layer, high heat

conductivity and insulating characteristics. The package contains the base with the recess for the chip, the lead frame, the insulating laying, and the cap.

The second variant of packages with flexible leads uses a thin aluminum wafer as a base. Contact pads and conductors outgoing to the cap attaching point are formed in the aluminum body by the two-side through anodization technique. The housing assembling consists in the mounting of the back plane to the base with heat-conducting glue, device mounting and cap gluing. Such the design excludes the electron-beam deposition of aluminum films.

The electrochemical aluminum technology [2] is also used for the leadless chip-carrier package production.

Fig. 1 shows the cross-sectional view of the aluminum package with the semiconductor chip. The package contains the base with the recess for the chip, the lead frame, the insulating laying, and the cap. The base, the insulating laying, and the cap are made of the aluminum alloy. The surface of all listed elements are coated with the $(10-50)\cdot10^{-6}$ m thick porous alumina layer. The chip is located in the base recess, and the chip contact pads are connected with the wire leads. The exterior lateral dimensions and the shape of the base, the insulating laying, and the cap are in close agreement and depend on the chip shape and dimensions. The lead frame is pressed to the base periphery by the insulating laying.

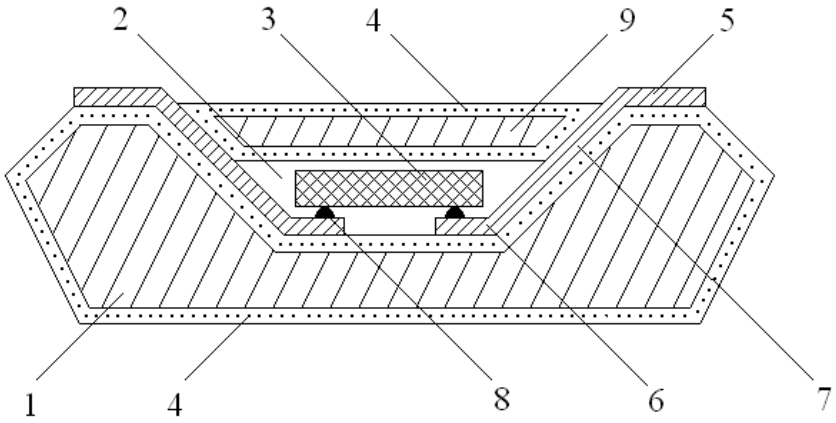

Fig. 1 Leadless chip-carrier package: (1) aluminum base; (2) recess for the chip; (3) chip; (4) porous alumina; (5) external contact pads; (6) internal contact pads; (7) conducting bridges; (8) ball-bearing leads; (9) aluminum cap

The technology of the aluminum package includes the batch manufacturing of the single structural components and the assemblage. To produce the package base, the blanks with the area divisible by *n* numbers of bases are selected, cleaned in trichloroethylene and isopropyl alcohol for 20 min, degreased in NaOH for 20 min, and decolorized in HNO_3 for 1 min. Then, the two-side photolithography is made, resulting in the openings for the narrow (~1 mm) separating gaps along the periphery of the bases to be formed and from one side for the recesses for chips as well. Next, the chemical milling in the solution of HCl and H_2O_2 for 10−15 min is performed and photoresist is removed in dimethylformamide. The array of the blanks for the package bases is produced.

This array then is subjected to the chemical polishing in $H_3HO_4+H_2SO_4+HNO_3$ for 10 мин and goes to the anodization in the 4% solution of the oxalic acid to form the $(10-50)\cdot10^{-6}$ m thick porous alumina layer. After rinsing in de-ionized water and drying,

the array is divided into the package bases by the mechanical removal (cutting down) of bridges at the base corners. The package laying and cap are produced by the similar batch method using only other photomasks. The lead frame is made of kovar by the batch method as well with the use two-side photolithography and chemical etching.

Terminals of the chip-carrier package are formed by the vacuum deposition technique and are brought out into the top side of the base through the lateral face. The use of the photolithography and deposition techniques allows 0.1 mm and less lead spacing to be organized. Mounting is made by the flip chip technique.

Fig.2 demonstrates the chip-carrier package with terminals outgoing to the bottom side of the base.

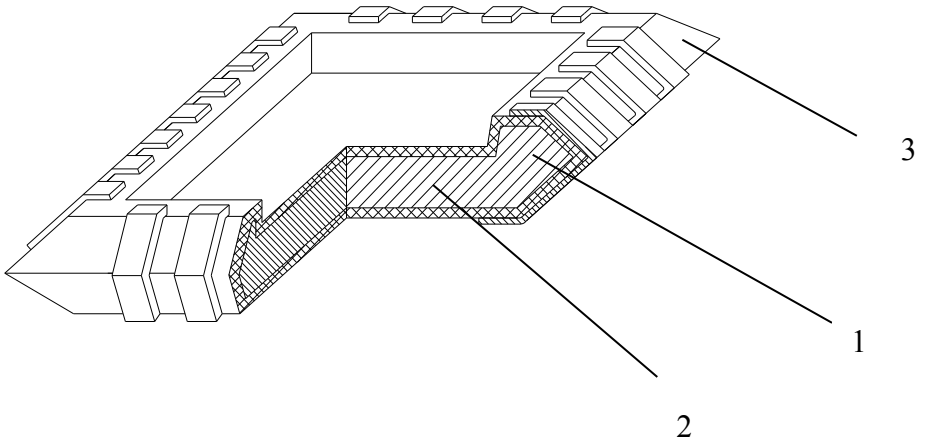

Fig. 2 Leadless chip-carrier package: (1) aluminum base; (2) porous alumina layer; (3) external contact pads

This variant of the package is also made by the above-mentioned technology. Terminals of the chip-carrier package are formed by the vacuum deposition technique and are brought out into the bottom side of the base through the lateral face. The use of the photolithography and deposition techniques allows 0.1 mm and less lead spacing to be organized. In this case mounting of chip is made using conventional wire bridges.

References:

[1] Lau J. H. and Lee S.-W. R. Chip Scale Package (CSP): Design, Materials, Processes, Reliability, and Applications. Published
by McGraw-Hill Professional, 1999, 564 pages.

[2] Sokol V., V. Shulgov V. Electrochemical Aluminium Oxide Technology of Electronic Devices Production / 51st Internationales Wissenschaftliches Kolloquium Technische Universität Ilmenau September 11 – 15, 2006, pp 327-328.

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