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A SUPERCONDUCTOR FLASH ANALOG TO DIGITAL CONVERTER

Taghrid Haddad, Alexander Scherer, Thomas Ortlepp

Institute for Information Technology, RSFQ design group,
Ilmenau University of Technology,
P.O. Box 100565, 98684 Ilmenau, Germany
taghrid.haddad@tu-ilmenau.de

ABSTRACT

This paper investigates the topology of a superconducting flash-ADC. Superconductive electronics is based on Josephson junctions and provides very high switching speed as well as very low power consumption. The Quasi-One-junction-SQUID is used as a comparator with the special feature of a period output characterisitc. A resistive network generates binary divided input currents for all bits. We study a special implementation of a 4 bit flash ADC. The results are obtained by numerical circuit simulations including the influence of thermal noise at an operation temperature of 4.2 Kelvin. We demonstrate the potential to provide a 4 bit resolution with a sampling frequency of 20 GHz. The circuit optimization is done with respect to a future circuit realization.

Index Terms— Analog-to-Digital converter (ADC), quasi-one-junction-SQUID (QOJS), superconducting quantum interference device (SQUID), single-flux quantum (SFQ), rapid single flux quantum (RSFQ).

1. INTRODUCTION

The Rapid Single Flux Quantum (RSFQ) electronics is the most promising quantum electronics [1]. It offers an intrinsic digital logic which represents the information by the presence or absence of a magnetic flux quantum $\Phi_0 = \frac{h}{2e}$ (Planck constant h and elementary charge e) in a superconducting loop. The extremely high sensitivity of a Superconducting Quantum Interference Device (SQUID) regarding magnetic flux makes it an outstanding detector device even for very low magnetic fields. It acts as a flux-to-voltage-converter. Generating the magnetic flux by a current I, it can be used as a current-to-voltage-converter, making it applicable for analog-to-digital-conversion.

The authors like to thank the Tishreen University in Syria for supporting this research.

2. ONE-BIT-QOJS-COMPARATOR

The QOJS [2] is a loop that consists of $L_1, L_{2a}, J_1, L_{2b}, J_2, J_{g2}$. The critical current of the one junction is much smaller than the other one. The Fig. 1 shows the circuit diagram of the investigated QOJS comparator. The current I_{IN} represent the analog input signal. With every clock pulse at the clock input, one of the two junctions J_2 or J_5 must switch. If the critical current of J_2 is exceeded at the moment of a clock pulse, J_2 switches and the SFQ-pulse is produced at the data output. If not, J_5 will switch and no SFQ-pulse is produced at the output. J_2 and J_5 build a comparator, which is controlled by the input current. J_2, L_3 and J_3 build a Josephson Transmission Line (JTL), which is used to transfer the output data to the next stage. J_5 is an escape junction and always switches when J_2 does not switch. In this case the flux quantum leaves the circuit across this junction. The switching of J_2 corresponds to logic 1 and the switching of J_5 corresponds to logic 0. For a linear input current ramp, the comparator reacts periodically with ranges of 0 or 1. Figure 2 shows the simulated switching probability of J_2 as a function of input current for three periods of a logical 1. From this figure one can see the following points, which must be optimized in the circuit:

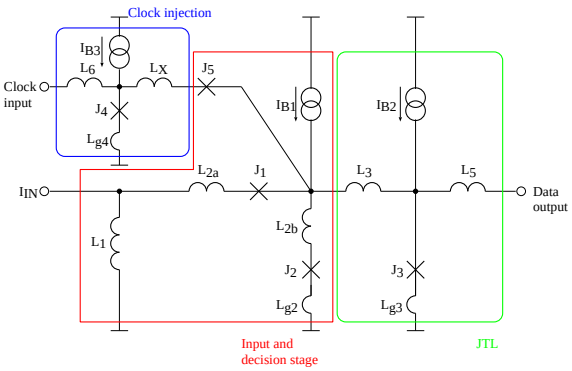

Fig. 1. Unoptimized 1-bit-QOJS comparator.

- Current ranges for 1 and 0 do not have the same width.

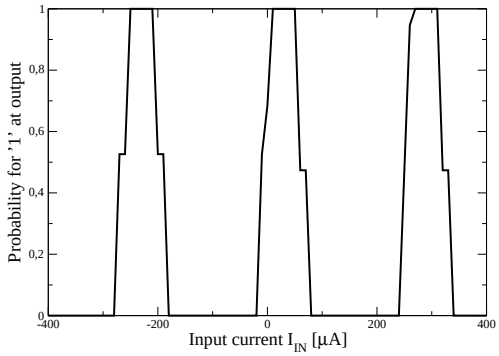

Fig. 2. Probability for 1 at the output of an unoptimized 1-bit-QOJS comparator as function of input current.

- The transition between 1 and 0 is not sharp. There is a plateau with a switching probability of 50%.
- The comparator must not be hysteretic (the current digitized value must not depend on the previous value).

Therefore it is good, if the comparator has the following properties:

1. The comparator must offer high sample rates to enable the digitization of analog signals with high bandwidth.
2. The sensitivity must be as good as possible, so the period of 1 and 0 must be as small as possible.
3. The convertible dynamic range of the analog signal must be as high as possible.
4. The current digitized value must not depend on the previous value (hysteresis free).
5. The transitions 1/0 and 0/1 must be sharp.
6. The periods of 1 and 0 must have the same width.

The first property is realized by the intrinsic speed of the RSFQ-logic and the second is limited by the thermal noise. Our first estimation result in a possible resolution of 15μA. Property 3 is limited by the maximum current, which can flow in the inductance L_1. In our case, this limits the input current to about 100 mA, because the produced magnetic field will affect the functionality of Josephson junctions at higher currents. Properties 4,5 and 6 will be realized in the opitimized version.

3. OPTIMIZED 1-BIT-QOJS-COMPARATOR

The final circuit of the 1-bit-QOJS-comparator (Fig. 1) was extended by a buffer stage, which prevents a double switching of J_4. This avoids a trapped flux quantum or an SFQ pulse to travel back across the clock input to the DC/SFQ-converter as shown in Fig. 3. The parameters of the input stage are chosen in a way, that the main part of the input current flows through the comparator junctions J_2 and J_5 and the minor part flows in inductance L_1. From this a high value of inductance L_1 and a junction J_1 with a relatively small critical current I_{c1} results. This junction is responsible for the periodicity of the input current. All currents, which flow through the junctions have an influence during the dimensioning process. Every current shows a periodic behaviour due to the periodicity of the QOJS. If the input current becomes too large, J_1 will switch and redistributs a fixed amount of the current to the inductor (the same part of I_{IN}, which flows through J_1, will be back in the branch after switching of J_1). So the whole circuit acts periodic with respect to the input current. The table 1 shows the parameter values of the optimized version, which are used for the circuit simulation. The plateau appears when the ring currents, which are produced by a switching of J_2 and J_4, are not enough to make J_1 to switch. This will also happen, when the input current through J_1 is close to its critical current. With the next clock pulse the current through J_2, J_4 will be very small so J_2 will react to this pulse with 0. The produced ring current of J_4 is enough now to make J_1 to switch, so the state of the previous clock pulse will appear again. In order to eliminate this plateau two ways were investigated:

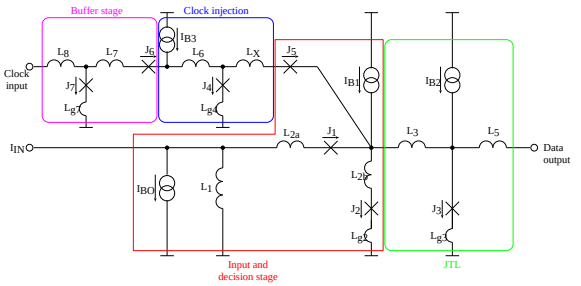

Fig. 3. Optimized 1-bit-QOJS comparator.

- First we tried to increase McCumber parameter β_c of J_1. Thereby the high dynamics of J_1 makes the current overshoot, if J_1 switches, to enter the critical range of the jump from $+I_{c1}$ to $-I_{c1}$ in the same clock cycle. With this idea the plateau can be reduced from 50μA to 30μA with $\beta_{c1} = 16$ and to 15μA using unshunted J_1. This leads to satisfied results when the clock frequency is 10 GHz, but with 20 GHz the results become not reliable.
- The better solution is to decrease the ring inductance of the path of the ring current of J_4 (I_{k4}), that $I_{k1} + I_{k4} \gg 2 \cdot I_{c1}$. But it is not enough that L_x, L_{2a} are reduced because L_1 can not be

Inductances	Values[pH]	Junctions	Values[μA]	Bias currents	Values[μA]
L_1	2	I_{c1}	150	I_{B1}	391.5
L_{2a}	0.2	I_{c2}	450	I_{B2}	150
L_{2b}	0.2	I_{c3}	250	I_{B3}	270
L_3	4.5	I_{c4}	250	I_{BO}	200
L_5	2.08	I_{c5}	225		
L_{g2}	0.198	I_{c6}	200		
L_{g3}	0.11	I_{c7}	250		
L_6	2				
L_x	0.2				
L_7	2				
L_8	2				
L_{g4}	0.12				
L_{g7}	0.12				

Table 1. Parameters of the optimized version.

reduced. The best solution is to increase the critical current of one of the two junctions J_1 or J_5. This leads to decrease the inductance of Josephson junction.

Figure 4 shows the simulation results of the probability of the optimized version with and without noise. From this figure one can see that the periods of logic 1 and 0 are nearly the same and the plateau was eliminated.

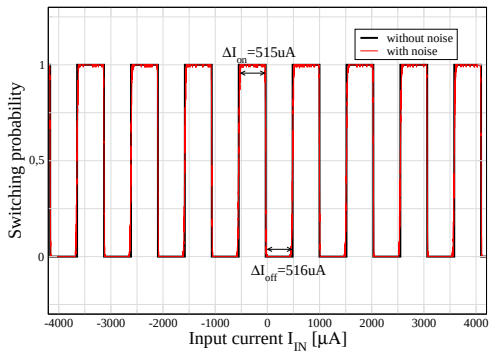

Fig. 4. Probability of an optimized 1-bit-QOJS comparator as function of input current with and without noise.

4. BUILDING A SUPERCONDUCTOR 4-BIT-FLASH-A/D-CONVERTER WITH QOJS-COMPARATORS

The Fig. 5 shows a superconductor 4-bit-flash-A/D-converter with four QOJS-cells, where the current distribution is made with the means of R/2R ladder. The analog input current I_{in} is divided by a factor of two after each of the n taps of the R/2R ladder and is applied to one of n (here 4) QOJSs [3]. The first QOJS-cell gets 2^{n-1} times the analog input current applied to the last QOJS-cell [4]. This distribution enable to use identical QOJS-cells for all bits. The output of the first comparator (QOJS) represents the least significant bit (LSB) and the last comparator generates the most significant bit (MSB). For the presented circuit, the comparator for the LSB gets half of the total input current and the MSB gets only 1/16 of the input current. The single QOJS cell has a resolution of 0.5 mA, which results in an LSB of 1 mA and MSB of 8 mA, respectively. All QOJS cells require a clock signal, which appears

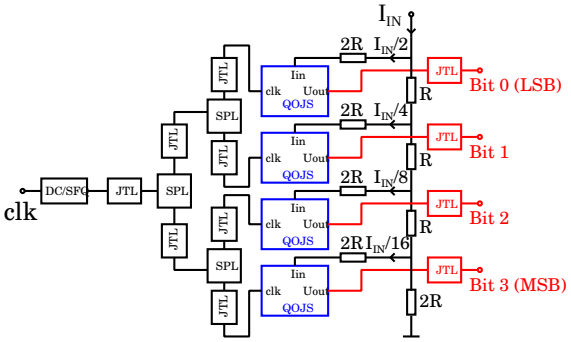

Fig. 5. Structure of 4-bit flash ADC. There are two inputs, one for clk-signal and the another for input current, which is used for the measurement, and four comparators outputs. JTL and splitters from RSFQ- cell library [5].

at the same time. An external clock generator is used to trigger a dc/SFQ-converter, resulting in a chain of single flux quantum (SFQ) pulses, which are synchronized to the external source. Splitter cells (SPL) are used to double the SFQ pulses. Each input SFQ pulse produces two output pulses, one at each output port. The splitters are used to generate a clock distribution network. All clock pulses must arrive simultaneously at the clock input ports of the four comparators (QOJSs). In order to realize this synchronization, a strong symmetry of all branches of the structure shown in Fig. 5

is required. The Josephson Transmission Lines (JTL) at the output are used for the stabilization and decoupling of the output ports. The digital information of four comparators results in a huge data volume at high sampling speed. There is no direct solution for a real time data storage. To solve this problem, fast on-chip data aquicition memory or decimation filters [6] can be connected to the comparators outputs. The data link between superconductor and semiconductor electronics is limited in speed and special output drivers [7] are required to allow a high volume data transfer from the superconducting flash-ADC to the data aquicition and processing computer.

5. SIMULATION RESULTS

If the comparators are not exactly adjusted, this will cause serious conversion errors. All 4 QOJS cells must have the 1/0 transition at $I_{in} = 0\mu$A and a ratio of $\frac{I_{on}}{I_{on}+I_{off}} = 50\%$. This can be adjustable by means of the currents I_{BO} and I_{B1} of every QOJS-cell. The simulation of the 4 bit flash converter was made without thermal noise. The Fig. 6 show the simulation results in the case, where the 1/0 transition of the 4-QOJS-cells does not happen correctly. In this case, we observe a big uncertainty during transition between all bits. This problem requires an accurate adjustment of the QOJS cell and of the R/2R ladder network. The

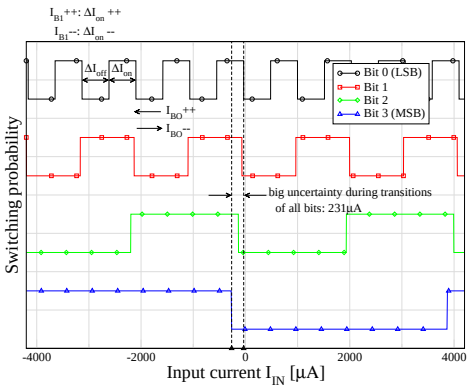

Fig. 6. Outputs of 4-bit flash ADC at $T = 0$K.

transient simulation of the 4-bit-comparators without noise and a clock frequency of $f = 10$GHz gives conversion errors (outlier) as shown in Fig. 7. The previous simulation was repeated with the same settings but with sine-wave input current as shown in the Fig. 8.

The figures 7 and 8 confirm the functionality of the flash-ADC with a clock frequency of $f_{clk} = 10$GHz and a resolution of four bits. This converter was also investigated at $f_{clk} = 20$GHz and the results confirm correct function of the flash-ADC, but for frequencies above $f_{clk} = 20$GHz the converter does not operate

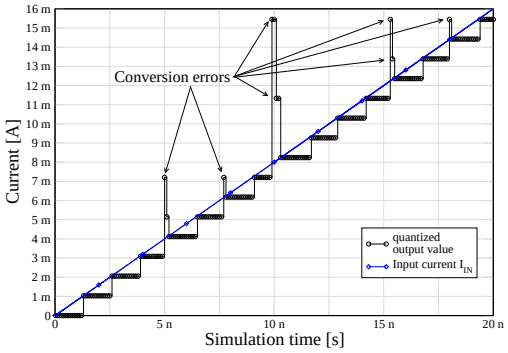

Fig. 7. Conversion results of the 4-bit-comparators at $T = 0$K, $f_{clk} = 10$GHz, input current is a linear ramp $0 - 16$ mA.

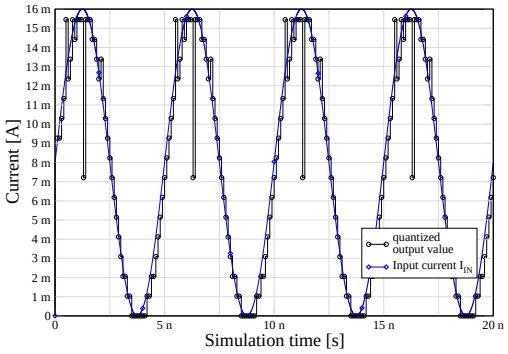

Fig. 8. Conversion results of the 4-bit-comparators at $T = 0$K, $f_{clk} = 10$GHz, input current is a sine wave with bias: $8mA \cdot \sin(2\pi \cdot 200MHz \cdot t) + 8mA$.

correctly.

6. CONCLUSION

The optimized version of the 4 bit flash A/D converter shows a good performance in circuit simulations for clock frequencies below 20 GHz. The hysteresis of the QOJS could be completely removed by reoptimization of the circuit parameters. The observed plateau at the 50 % level is a characteristic feature for all kind of Josephson based comparator circuits. During the optimization process, we payed special attention to eliminate this feature for the preset design. Since the QOJS comperator can sometimes reflect the trigger pulse, an extra buffer stage was introduced before the comparator stage. This is required to avoid any back-action of such a reflection to other bits of the flash A/D converter via the clock distribution network.

After a final approval of the circuit architecture by further simulation studies, we plan an implementation

in the mature RSFQ fabriaction process of FLUXONICS Foundry [5]. In parallel we will be an investigation of the maximum clock frequency as well as different possibilities for the readout of the digital output data (e.g. by means of shift registers or decimation filters. The characteristic parameters of the A/D converter such as integral and differential nonlinearity, effective number of bits and SFDR will be investigated in circuit simulations as well as by experiments.

7. REFERENCES

[1] V. V. Zhirnov et al., "Emerging research logic devices," *IEEE Circuits & Devices Magazine*, vol. 21, pp. 37–46, May/June 2005.

[2] T. Harnisch, F. H. Uhlmann, H. Toepfer, D. F. Moore, A. J. Pauza, and K.Lamacraft, "Modeling of an adc based on high-tc qojs comparators," *IEEE Trans. Appl. Superconduct.*, vol. 5, pp. 2628–2631, June 1995.

[3] P. Bradley and H. Dang, "Design and testing of quasi-one junction squid-based comparators at low and high speed for superconductor flash a/d converters," *IEEE Trans. Appl. Superconduct.*, vol. 1, pp. 134–139, September 1991.

[4] O. A. Mukhanov et al., "Superconductor analog-to-digital converters," *proceedings of the IEEE*, vol. 92, pp. 1564–1584, October 2004.

[5] *www.fluxonics-foundry.de*.

[6] T. Stoyadinova, I. Buzov, K. Filipova, V. Mladenov, T. Ortlepp, "Development of VHDL-models for transient simulation of komplex asynchronous RSFQ circuits," *conference iwk 2009*, September 2009.

[7] T. Ortlepp, S. Wuensch, M. Schubert, P. Febvre,B. Ebert, J. Kunert, E. Crocoll, H.-G Meyer, M. Siegel and F.H. Uhlmann, "Superconductor-to-semiconductor interface circuit for high data rates," *IEEE Transactions on Applied Superconductivity*, vol. 19, pp. 28–34, February 2009.