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DESIGN, FABRICATION, AND TESTS OF RSFQ CIRCUITS BASED ON THE FLUXONICS FOUNDRY

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ABSTRACT

The paper provides an overview of the design and fabrication process of Rapid Single Flux Quantum (RSFQ) circuits [1] and a demonstration of the established integrated framework of the FLUXONICS Foundry [2]. Test circuits demonstrate the integration of functional elements into more complex devices. The circuits were extensively tested, including an on-chip 30 GHz test using a ladder-type clock generator, as well as by bit error rate measurements. The results presented here show the potentials and the reliability of the European FLUXONICS Foundry for the design and fabrication of robust RSFQ circuits for end-users in research and industry.

This work has been supported by the European FP7-Project S-PULSE [3].

Index Terms - RSFQ, Josephson Junction, Superconductor Electronics, Fabrication, Foundry

1. INTRODUCTION

The today's life is unimaginable without electronic devises. The development of semiconductor electronics is directed to higher integration and speed. The clock speed of semiconductor microprocessors seems to reach a status of saturation in the range of 3-4 GHz. Heat dissipation problems are the main reason for this limitation.

The RSFQ electronics, based on effects in superconductor materials, offers high speed together with very low power dissipation. So these circuits can be operated at several tens of GHz without the limitation of heat. The availability of effective cryo cooling systems has improved the opportunity to build easy-to-use complex superconductor electronics systems [4].

2. RSFQ STANDARD PROCESS

In the fabrication process of RSFQ circuits equipment and technologies like thin film deposition and patterning are used comparable to semiconductor processes.

The process is the standard for RSFQ at IPHT since several years [5] and certified by the DIN EN ISO9001. Information of the current standard process RSFQ1D is available for circuit designers including design rules on an internet platform [2].

A cross-section of the typical elements of the RSFQ circuitry is shown in figure 1 as schematic and in figure 2 as REM picture.

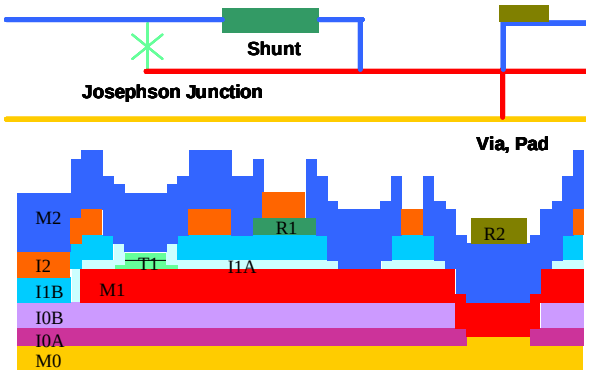

Fig.1: Schematic cross-section

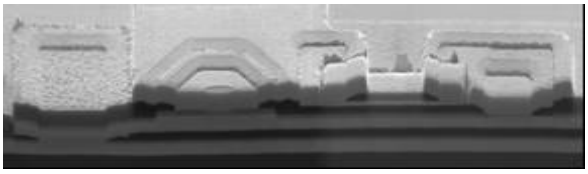

Fig.2: REM picture of the cross-section

The topological structures are defined with photolithography engineering on thermally oxidized

Si wafers of four inch diameter. The used contact lithography defines the overlap from layer to layer of 2.5 µm. In table 1 all layers and film thicknesses are listed.

Layer name	Layer function	Thickness [nm]	Material
R2	Bond pad	50	Au
M2	Upper Wiring	350	Nb
I2	Insulation	150	SiO
R1	Resistor	80	Mo
I1B	Insulation	150	SiO
I1A	Insulation	70	Nb_2O_5
T1	Josephson Junction	60 12 30	Nb Al_2O_3 Nb
M1	Lower Wiring	250	Nb
I0B	Insulation	200	SiO
I0A	Insulation	50	Nb_2O_5
M0	Ground plane	200	Nb

Tab. 1: Layer description of the Process RSFQ1D

The physical properties are determined by the materials. Niobium (Nb) is used as superconductor with a critical temperature T_C of 9.2 K. The Nb is deposited by dc magnetron sputtering and patterned by reactive ion etching (RIE) in CF_4 plasma. For the insulation between the niobium layers Nb_2O_5 and SiO are used. The Nb_2O_5 insulation is made by anodization [6] up to a voltage of 25 V. The insulation is reinforced by two evaporated SiO layers. Holes for connection through the insulation are opened by lift-off. The electrical active functional element is the Josephson junction (JJ). The JJ is a very thin insulator between superconductor layers and works as tunneling barrier. In the RSFQ standard process the tunnel barrier consist of Al_2O_3. This so called trilayer [6] is a stack of Nb, Al, Al_2O_3, and Nb. The trilayer is deposited without vacuum interruption. The thickness of Al_2O_3 is determined by oxidation of the Al film at room temperature in a pure oxygen atmosphere. The oxide thickness is in the range of one nanometer. The area of JJ is defined by following complete anodization of the trilayer counter electrode up to a voltage of 35 V. For the anodization all structures in the ground plane and in the lower wiring layer have to be connected to the anodization terminal. For the not grounded structures of the circuit this is done with additional wires, which are removed by a cut etch step using RIE in CF_4 plasma. The density of the critical current J_C of the trilayer is 1 kA/cm^2 in the standard process. Resulting from the contact lithography the smallest junction area is 12.5 µm^2. The typical characteristic of such a JJ is hysteretic. The RSFQ electronics need a non hysteretic function. A shunt resistor suppresses the hysteresis. The resistor layer is consists of molybdenum (Mo) and has to be protected by SiO against air and environmental influences. The sheet resistance of the Mo layer is 1 Ohm. The Mo film is sputtered and patterned by lift-off. For the RSFQ electronics the inductors are important passive elements. These inductors are defined by the thickness of the Nb layers and the insulation layers. The bonding pads are covered with gold (Au) to improve the bonding conditions..

3. PROCESS CHARACTERISATION

Each fabricated wafer has to pass a characterization procedure. This procedure consists of measurement of critical currents I_C, the resistances, the inductances and their tolerances. If all parameters are inside the specification, a functional RSFQ test completes the characterization procedure. The specification of parameters and tolerances are listed in table 2.

Parameter	Nominal Value	Tolerance in ± %		
		Total	On Wafer	On Chip
Critical current density J_C	1kA/cm^2	20	15	5
Sheet resistance R_{Square}	1 Ohm	20	10	5
Inductance M1-M0	0.52 pH	10	5	2
Inductance M2-M1	0.64 pH	10	5	2
Inductance M2-M0	0.81 pH	10	5	2

Tab. 2: Specification of parameters and tolerances

Unified test circuits are placed on each wafer for the measurement of parameters. These test structures consist of resistors, unshunted JJ and shunted JJ. The value of I_C and the shrink of critical dimensions can be calculated from the measurement results. Other measurements are done for the normal resistance R_N of the JJ and for the sub-gap resistance R_S at 2 mV. A product I_CR_N more than 1.4 mV and a ratio R_S/R_N more than 20 are parameters for high quality JJ. The spread of the I_C can be measured with arrays of 200 JJ. SQUID structures with different layer configurations exist for the measurement of the inductances.

If all parameter tests have been passed follows the function test of an unified RSFQ circuit. The test circuit is a configuration of a DC/SFQ converter, a Josephson transmission line (JTL), and a SFQ/DC converter. Figure 3 shows this test circuit.

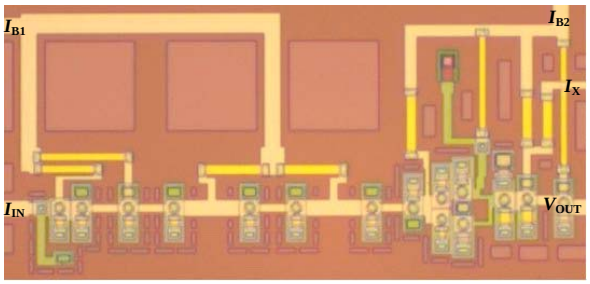

Fig.3: Picture of the test circuits

The test circuit has terminals for bias currents I_{B1}, I_{B2}, I_X, input current I_{IN} and output voltage V_{OUT}. A triangle form input current I_{IN} clocks the circuits. The DC/SFQ converter switches on the increasing slope. Figure 4 and 5 show the behavior of the circuits for input current I_{IN} amplitudes corresponding to one and four magnetic flux quantum Φ_0.

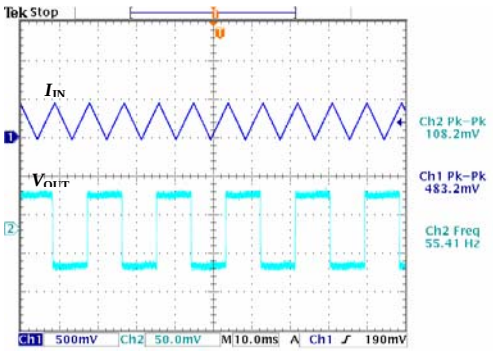

Fig.4: Function of the test circuit with I_{IN} corresponding to one Φ_0 shows one switch of V_{OUT} on each increasing slope of I_{IN}

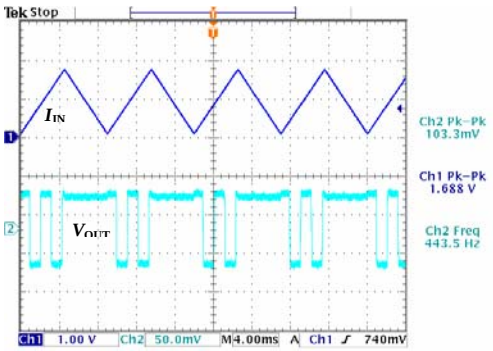

Fig.5: Function of the test circuit with I_{IN} corresponding to four Φ_0 shows four switches of V_{OUT} on each increasing slope of I_{IN}

4. TEST OF RSFQ CIRCUITS

The bit error rate (BER) is an important parameter for digital circuits and gives information about the reliability of complex circuits. As example the BER of the circuit in figure 6 was measured in dependence of the two bias currents I_{B1} and I_{B2}.

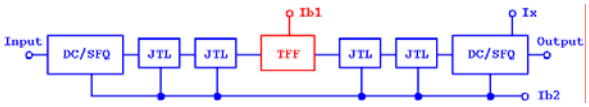

Fig.6: Schematic of the test circuits for the 2D BER.

This 2D BER measurement was performed in a DSP controlled test set-up. The input I_{IN} was fed by a triangle form input current with an amplitude corresponding to one Φ_0. The measurement set-up checks the correct output voltage behavior. The number of errors is notified. The measurement time of 0.2 s and the frequency of 50 kHz correspond to 10,000 tests for each point. In this case zero error means a BER of better than 10^{-4}. Figure 7 shows a plot of the 2D BER depends of the two bias currents.

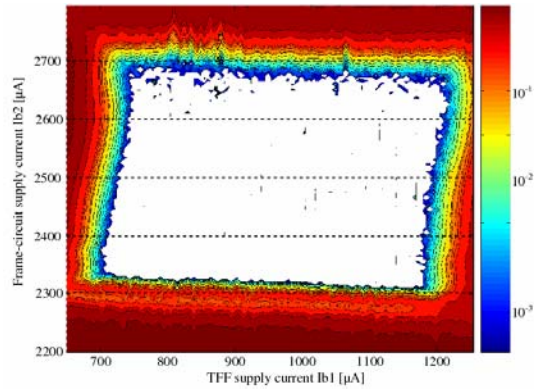

Fig.7: Result of the 2D BER measurement

In the white area the BER is lower than 10^{-4}. The white rectangle box is the expected figure.

The previously described tests are at low frequencies in the kHz range. The destined frequency range for RSFQ electronics is in the range of tenth of GHz. Tests in this range is difficult. They need very expensive equipment and the complete set-up has to be optimized for this frequencies. For general tests of the function of circuit elements the on-chip test is a good alternative. Such a test was implemented on a circuit for pseudo high frequency tests. The schematic is shown in figure 8.

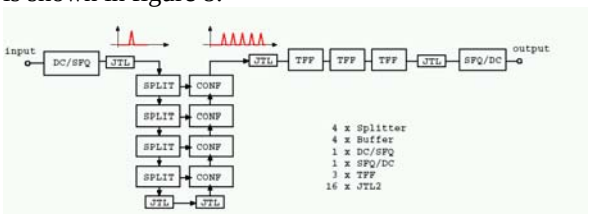

Fig.8: Schematic of the pseudo high speed test circuit

The DC/SFQ converter input follows a cascade of four splitters and four confluence buffers. The cascade generates by each input signal sequences of five single flux quantum (SFQ) pulses. This cascade is called ladder-type generator. The distance of pulses is determinate by delays inside the cascade and corresponds to a frequency of 30 GHz. This high frequency sequences recur with the input clock

frequency in the range of kHz. For each clock event at the input the measurement in the kHz range at the output shows the circuit function corresponding to five SFQ pulses. The device under test is a cascade of three toggle flip-flops (TFF). This TFF cascade is fed by the ladder-type generator and is read out by a SFQ/DC converter. Because the SFQ/DC converter operates also like a TFF, the whole circuit is a 4 bit ripple-counter. The output signal behavior is a 16 bit pattern in the kHz range and can be calculated. Figure 9 shows the simulated wave form.

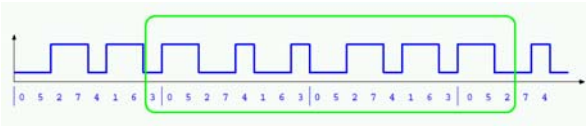

Fig.9: Simulated output signal of the pseudo high speed test circuit

The measured wave form in figure 10 shows this predicted pattern.

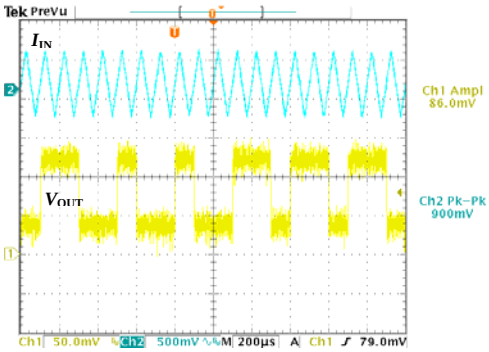

Fig.10: Measured output signal of the pseudo high speed test circuit

The TFF cascade operates internally correct at 30 GHz. The complete test circuit is build of 99 Josephson junctions.

5. FLUXONICS FOUNDRY

The presented RSFQ circuits have been designed, fabricated and measured in the FLUXONICS foundry. The FLUXONICS Foundry [2] for RSFQ circuits was established by the European FLUXONICS network. This Foundry provides a complete design and fabrication infrastructure including a library of designs for basic gates, and design support. The fabrication is based on a DIN EN ISO9001 certified circuit fabrication process associated with an extensively tested cell library of basic RSFQ gates. The library serves as a key access to the field of RSFQ electronics and provides also general as well as detailed descriptions for the superconductor electronics technology. The cell-based design is the most straightforward solution for a standard design process in digital electronics. The cell library includes the interface cells between RSFQ and semiconductor electronics as well as all general cells for the transmission, distribution and combination of SFQ pulses. All cells have been analyzed experimentally and can be integrated into larger circuits without further optimization.

6. OUTLOOK

The world wide direction of the development of fabrication processes for complex RSFQ circuits is to higher integration level and faster operation speed. The higher integration level corresponds to smaller structures. The higher operation speed needs higher current densities resulting also in smaller structures. These two aspects presage the future developments of the RSFQ process of the FLUXONICS Foundry. The change from contact lithography to wafer stepper based projection lithography will be done in the near future. First JJ with sub-micron dimensions have been fabricated and successfully tested [7]. The long term improvement will be the increase of the critical current density.

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