07 - 10 September 2009

PROCEEDINGS

54. IWK

Internationales Wissenschaftliches Kolloquium
International Scientific Colloquium

Information Technology and Electrical Engineering - Devices and Systems, Materials and Technologies for the Future

Faculty of Electrical Engineering and Information Technology

TECHNISCHE UNIVERSITÄT
ILMENAU

Impressum

Herausgeber: Der Rektor der Technischen Universität Ilmenau
Univ.-Prof. Dr. rer. nat. habil. Dr. h. c. Prof. h. c.
Peter Scharff

Redaktion: Referat Marketing
Andrea Schneider

Fakultät für Elektrotechnik und Informationstechnik
Univ.-Prof. Dr.-Ing. Frank Berger

Redaktionsschluss: 17. August 2009

Technische Realisierung (USB-Flash-Ausgabe):
Institut für Medientechnik an der TU Ilmenau
Dipl.-Ing. Christian Weigel
Dipl.-Ing. Helge Drumm

Technische Realisierung (Online-Ausgabe):
Universitätsbibliothek Ilmenau
ilmedia
Postfach 10 05 65
98684 Ilmenau

Verlag: isle
Verlag ISLE, Betriebsstätte des ISLE e.V.
Werner-von-Siemens-Str. 16
98693 Ilmenau

ISBN (USB-Flash-Ausgabe): 978-3-938843-45-1
ISBN (Druckausgabe der Kurzfassungen): 978-3-938843-44-4

Startseite / Index:
http://www.db-thueringen.de/servlets/DocumentServlet?id=14089

ASCERTAIN OF THE LOCAL OPTOELECTRONIC SENSITIVITY AND BANDWIDTH OF INTEGRATED ANALOG CMOS PHOTODIODES

H. Luo / U. Ricklefs / M. Bensch

FH Giessen-Friedberg, University of Applied Sciences, Wiesenstrasse 14, D-35390 Giessen,
huanpingl@yahoo.de

ABSTRACT

The optoelectronic behaviour of integrated photodiodes on CMOS ASICs depends on wavelength and structure. In this paper integrated stripe-shaped CMOS photodiodes are described, that are used as image sensor elements with a high optoelectronic sensitivity and analog bandwidth. The geometry of shallow photodiodes in a n-well on a p-substrate is examined. In order to determine an optimal structure the photodiodes have different geometry and distance. All photodiodes were integrated on a single chip in a 0.5 µm mixed signal standard CMOS process (AMIS). By modification of a microscope, it was possible to produce a small spot with 1 µm in size ontop of the photodiodes to measure the local sensitivity.

1. INTRODUCTION

CMOS-technology allows highly complex and dense electronic circuits. In order to build smart sensors, sensorelements and electronic circuits could be integrated on the same application specific integrated circuit (ASIC). In optoelectronic applications it is possible to integrate photodiodes as well as their electronic for evaluation on the same customized ASIC (OPTO-ASIC).

OPTO-ASICs have some advantages in comparision to CCD/CMOS-cameras [1]. If photodiodes and their evaluation electronics are integrated on an ASIC, then there will be nearly no delay time between image capturing and generated output signal. In CCD/CMOS cameras based on arrays or line sensors the delaytime takes at least the image capturing time. So with these cameras high dynamic measurements could not be carried out. The next advantage to OPTO-ASICS is, that there is nearly no limitation belonging to the geometry and arrangement of the sensor elements and their corresponding electronics.

A p-n-junction is formed when p-type and n-type semiconductor material come into contact. The junction and the associated depletion layer of a photodiode play the main role in detecting photons by creating a photocurrent. The main current is generated in the depletion layer, wheras a smaller and much slower part of the current is generated outside of this layer in a range within the recombination length of the electron-hole pairs.

Simple photodiodes are implemented as deep wells in bulk silicon. Very often the bulk material is p-type doped whereas the deep well is n-type doped. The so created p-n-structure acts as diode and can be used as photodiode. The width of the depletion layer of this structure is small (typically in the range of microns). The situation for current generation is different at the side and in the inner region of the diode. Radiation incident on the inner region (fig. 1) has to cross a homogeneous doped region until it reaches the depletion region, where the generated electrons and holes are detectable. So the sensitivity of these structures for the generation of a photocurrent under normal conditions is low. Furthermore, because a part of the current is generated outside the depletion layer, these diodes are slow. At the side region of the diode the optical path of the radiation within the depletion layer is long. So the expected sensitivity should be higher.

In order to increase the sensitivity and bandwidth of these diodes so called PIN-structures are used. There are some customized OPTO-ASIC-processes belonging to these structures. But these processes are much more expensive than standard analog CMOS processes are. So the goal is to work with standard CMOS processes instead of PIN-CMOS processes and to increase the photoelectric sensitivity and bandwidth of standard CMOS photodiodes by structuring the geometry of integrated photodiodes.

In order to increase the bandwidth of CMOS-photodiodes it´s a common technique to use the described simple diodes only for separation purposes. If this diode is reverse biased, the inner area of the deep well is geometrically and electronically separetad from the surrounding. In the case of the common p-type bulk material the substrate is connected to Vss whereas the inner area is connected to Vdd. So the photocurrent generated in that diode is shorted.

In the discussed case (p-type substrate with an integrated deep n-type well) a number of p-type doped shallow wells could be integrated in the inner area of this deep well. This p-type doped shallow wells in conjunction with the n-type doped deep well create diodes that could be used as photodiodes. We designed and tested a number of different types of photodiodes (deep well, well in a well, different geometries) and discuss the results.

The studies are carried out with an AMIS 0.5 µm analog CMOS process.

2. THEORY

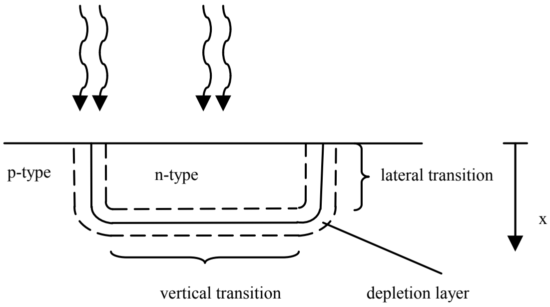

Figure 1 geometry

Diffused deep wells consist of more or less homogenuously doped material (fig 1, n-type doped material in p-type doped substrate). By physical processes a depletion layer is build at the layer between the doped well and the oppositely doped surrounding material. Certainly the boundaries are not as sharp as sketched in fig. 1 and will be different at the vertical and the lateral transition.

Normally for a certain CMOS-process it´s unknown, how weak or strong the transition from p-type to n-type really is. But its possible to do some rough calculations about the width of the depletion layer.

The depletion layer is extended to a small width into the strong doped material. The total width of the depletion layer is defined by the low doped region,

$$d_j = \sqrt{\frac{2\varepsilon_0\varepsilon_r(N_D + N_A)(U_D - V)}{e \quad N_D \times N_A}} \qquad (1)$$

with the voltage of diffusion U_D and the thermal voltage V_T

$$U_D = V_T \ln\left(\frac{N_D \times N_A}{n_i^{\,2}}\right)$$

For a silicon p-n junction with a donator concentration N_D and an acceptor concentration N_A at the temperature T d_j is calculated (not biased) as

N_D= 2E17cm-3 and N_A= 2.5E15cm-3

T= 300 K

d_j = 0.623 µm

Only a part of the photons incident on silicon will be transmitted and will generate electrons and holes inside the silicon. Only those charges generated inside or close to the depletion layer will cause a photocurrent.

Silicon absorbs the incident radiation. So the density of the radiational power p(x) will strongly decay in the depth of the silicon. This decay could be described by Lambert Beers Law with α as coefficent of extinction:

$$p(x) = p_0 \cdot e^{-\alpha \cdot x}$$

If in the region of the lateral transition the depletion layer doesn´t start at the surface, the incident radiation first has to cross a homogenuous charged region. Therefore this radiaion has to travel a much longer optical path until it reaches the depletion layer than radiation incident in the vertical transition region does. Additionally, the radiation reaching the space charge layer after crossing the well is much lower than at the surface. So, the sensitivity in both areas should be different.

Because α depends on the desired wavelength, the photocurrent should do as well.

3. EXPERIMENTAL SETUP

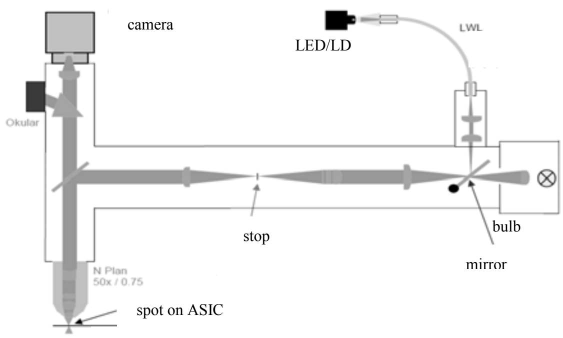

Figure 2 Optical path of Leica DMLM with modifications

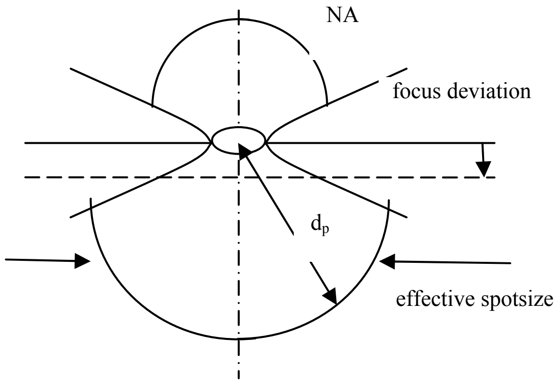

Figure 3 effective spotsize

Some smaller modifications are made at a Leica DMLM (fig. 2) with motorized stage. Limited by diffraction and quality of the microscopical imaging a small spot is imaged onto our testsamples. With this experimental setup, the local sensitivity of integrated photodiodes is measured.

The spot should be as small as possible - diffraction limited - ontop of the ASIC. For mechanical reasons the maximum magnification is 50:1. With higher magnifications the working distance of our objectives is too short. This led to collisions with the bond wires of the ASIC. So, the imaged spot on top of the photodiodes caused by diffraction has a diameter of approximately 1 µm (λ = 600 nm). Its smaller for shorter wavelengths.

The objective of the microscope has a large numerical apertur (A_N = 0.75; fig. 3). For this reason the effective spotsize will increase by the depth of penetration d_p:

$$d_p = 1/\alpha$$

At a wavelength λ of 800 nm the depth of penetration amounts 10µm (λ = 500nm: 0.78µm; λ = 400nm: 0.1µm). Therefore, the local resolution will be worse at longer wavelenths. At wavelengths smaller than 600 nm the depth of penetration is less than 1 µm. With this the effective spotsize at λ = 600nm increases to approximately 2 µm (λ = 500nm: 1.5 µm).

The surface of a OPTO-ASIC is non-planar. The wired conections show a z-deviation of round about 0.5 µm. The mechanics of our standard z-stage doesn´t allow to follow the profile of the surface. So, this leads to an additional increase of the spotsize of 1 µm in diameter in that plane. As long as the measurements are done in the plane of the photodiodes this has no effect. So, before starting a measurement the surface is adjusted relative to some plane reference points ontop of the photodiodes. The photodiodes lie more or less in the same plane. The mecahnical stability is very critical at that point. Our measurements show, that it is nearly impossible to scan larger areas.

As lightsource singlemode (in some cases multimode) fibres are used in combination with LD/LED of different wavelengths. The lightsources are modulated at low frequencies. The photocurrent is detected by a Lock In Amplifier SR830. The experiment is running under the control of MATLAB with implemented C-DLLs. The experiment is supervised by a camera. So, its possible to localise the actual position of the laserspot relative to the position of the ASIC. The OPTO-ASIC is electronical connected and shielded by a PCB (fig. 4). The repeatability of the stage is within one micron.

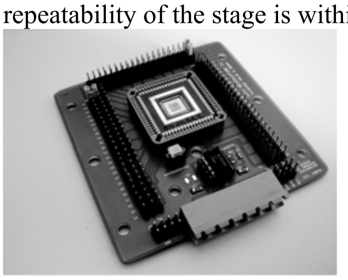

Figure 4 OPTO-ASIC with reference photodiode and I/U- amplifier on PCB

4. EXPERIMENTAL RESULTS

Fig. 5a shows the principle setup of one type of integrated photodiode. Other types of integrated photodiodes show simillar results. As could be seen (fig. 5b), the sensitivity in the area of the vertical

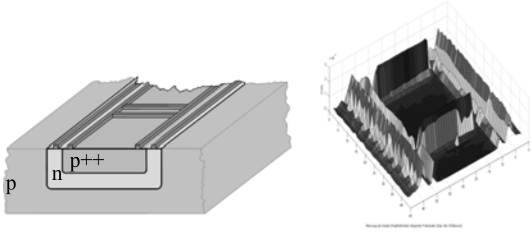

Figure 5a Principial structure,
Figure 5b local sensitivity

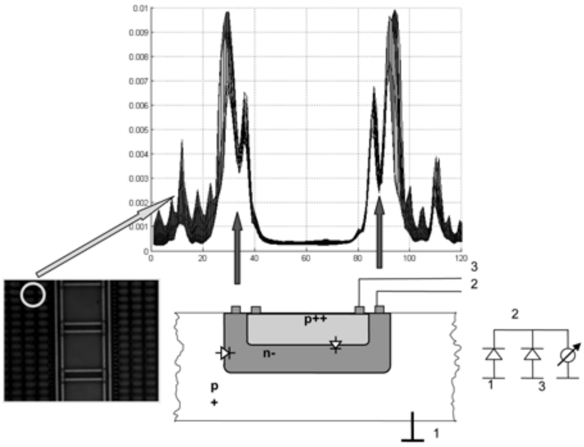

Figure 5c "horizontal view" to the data, localisation of the highest sensitivities, width of the depletion layer and shadow of the wires

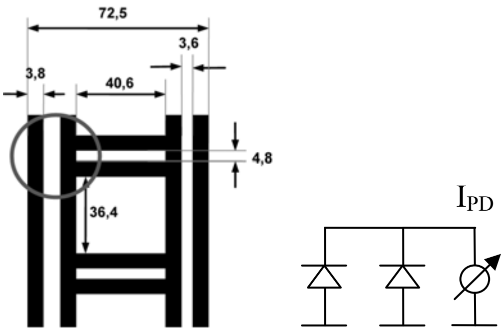

Figure 6a,b inner and outer PD parallel, wires

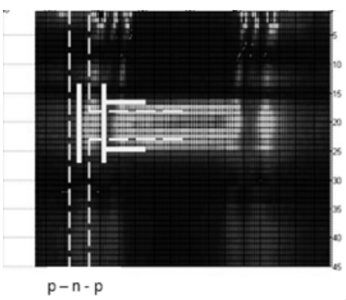

Figure 6c local sensitivity inner and outer PD transmission is extremly low. The sensitivity in the range of the lateral transmission nearly reaches the sensitivity of PIN-photodiodes similar to the very common BPW34. The sensitivity in the region of the substrat is caused by the opticaly non closed metal layer ontop of the surface. The photocurrent generated in this region is slow. It is generated within the diffusion region.

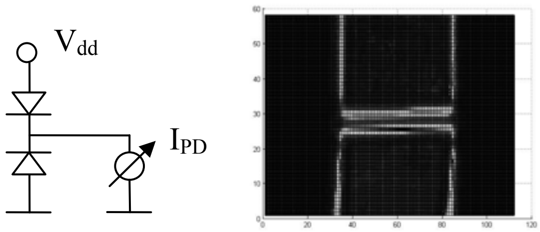

Figure 6d Inner PD isolated

Fig. 6 shows the influence of the reverse bias voltage on the width of the depletion layer and the isolation of the inner photodiode by short circuited photocurrent of the outer photodiode (fig. 6c, 6d).

With a bias of V_{dd} the width of the depletion layer reduces to approximately 1 µm. Non biased it has a width of about 3 microns. In a typical later application the photodiodes will be biased by about $V_{dd}/2$. So in these applications we expect a width of 2 µm.

Within the depletion layer the charge carrier are accelerated by the internal electrical field [2, 3]. So these so called drift carriers are fast. Within the recombination length around the depletion layer the carriers see no electrical field. These carriers are driven by diffusion. They are slow. In order to get fast diodes, the contribution of slow carriers to the total photocurrent should be small. The main contribution to the bandwidth of the photodiode is given by the capacity of the diode. This capacity is determined by the area A_j, the length of the border of the diode and the reverse bias U_D. The capacity of the border of the diodes is in the range of 10% of $C_j(0)$. The area of the diodes should be as small as possible and the bias U_D as high as possible.

$$C_j(0) = \frac{\varepsilon_0 \varepsilon_r A_j}{d_i}$$

d_j width of the depletion layer.

$$C_j(U) = \frac{C_j(0)}{\sqrt{1 - \frac{U}{U_D}}}$$

Our diodes show a capacity of approximately 16 pF. This fits well with the capacity caused by geometry. The measured bandwidth agrees well with the simulation where we simply replace the photodiode by this capacity.

With different wavelength (fig. 7) we see a strong change in the width of the active region. At long wavelengths this is caused by the increasing effective spotsize. Objectives of microscopes are designed for certain wavelengths. So we believe that the increased width at short wavelengths is caused by the degree of color correction of the objective at that wavelengths.

The simple calculation (1) of the width of the depletion layer seems to be half the measured value (fig. 7b, λ = 470 nm, measured value ca. 5 µm/2) . At higher voltages the width get smaller (fig. 6d).

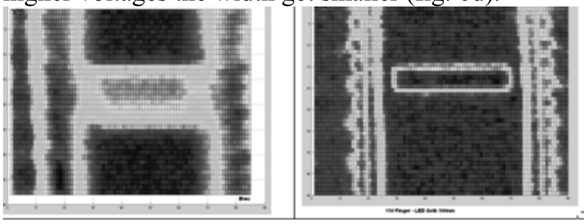

Figure 7a,b blue, yellow

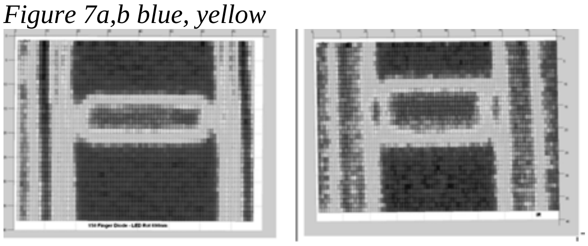

Figure 7 c,d red, infra red

5. CONCLUSION

Photodiodes generated by standard CMOS-processes show a similar sensitivity in the area of the lateral transition as PIN-diodes do. In the region of the vertical transition the sensitivity is low. With this technology the width of the sensitive layer at working voltages is about 2 µm. The bandwidth of the photodiodes is defined by the capacity caused by the area, the border of that area and the reverse biased voltage. Most of these investigations are promoted by the HessenAgentur (HA-Proj.-Nr.: 90/05-0; Flexibler optoelektronischer Korrelations-Geschwindigkeits-sensor mit integrierter Photodiodenzeile).

6. REFERENCES

[1] Dyck, R. H.; Weckler, G. P.: CMOS Integrated Array of Silicon Photodetectors for Image Sensing In: IEEE Transactions on Electron Devices, VOL.ED-15(4), 1968

[2] Radovanovic', Saša; Annema, Anne-Jahan; Nauta, Bram: High-Speed Photodiodes in Standard CMOS Technology. Nederland: Spring. 2006

[3] Schanz, Michael: Eindimensionale CMOS Bildsensorik mit integrierter Signalverarbeitung, Dissertation, Gerhard - Mercator - Universität - Gesamthochschule Duisburg, 9. Juni 1998