51. IWK

Internationales Wissenschaftliches Kolloquium
International Scientific Colloquium

PROCEEDINGS 11-15 September 2006

FACULTY OF ELECTRICAL ENGINEERING AND INFORMATION SCIENCE

INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING - DEVICES AND SYSTEMS, MATERIALS AND TECHNOLOGIES FOR THE FUTURE

Startseite / Index:
http://www.db-thueringen.de/servlets/DocumentServlet?id=12391

TECHNISCHE UNIVERSITÄT
ILMENAU

Impressum

Herausgeber: Der Rektor der Technischen Universität Ilmenau
Univ.-Prof. Dr. rer. nat. habil. Peter Scharff

Redaktion: Referat Marketing und Studentische Angelegenheiten
Andrea Schneider

Fakultät für Elektrotechnik und Informationstechnik
Susanne Jakob
Dipl.-Ing. Helge Drumm

Redaktionsschluss: 07. Juli 2006

Technische Realisierung (CD-Rom-Ausgabe):
Institut für Medientechnik an der TU Ilmenau
Dipl.-Ing. Christian Weigel
Dipl.-Ing. Marco Albrecht
Dipl.-Ing. Helge Drumm

Technische Realisierung (Online-Ausgabe):
Universitätsbibliothek Ilmenau
ilmedia
Postfach 10 05 65
98684 Ilmenau

Verlag:
Verlag ISLE, Betriebsstätte des ISLE e.V.
Werner-von-Siemens-Str. 16
98693 Ilrnenau

ISBN (Druckausgabe): 3-938843-15-2
ISBN (CD-Rom-Ausgabe): 3-938843-16-0

Startseite / Index:
http://www.db-thueringen.de/servlets/DocumentServlet?id=12391

51st Internationales Wissenschaftliches Kolloquium
Technische Universität Ilmenau
September 11 – 15, 2006

D. Kirsten / S. Richter / Dr. D. Nuernbergk / St. Richter

An EEPROM cell for automotive applications in PD-SOI

1. ABSTRACT

The feasibility of EEPROM memories in SOI process technologies has been proven [1]. It has also been shown that known data retention problems at high temperatures caused by leakage currents can be solved without extra circuitry [2]. In this paper results of EEPROM cell matrix measurements of two different cell designs regarding functionality and reliability will be presented. The process technology used is a 1.0 µm partially depleted SOI technology.

2. SOI TECHNOLOGY

Due to low leakage currents, Silicon-on-Insulator (SOI) technologies are well suited for high temperature circuit design. The reduction of leakage currents is especially important in large repetitive structures like memories.

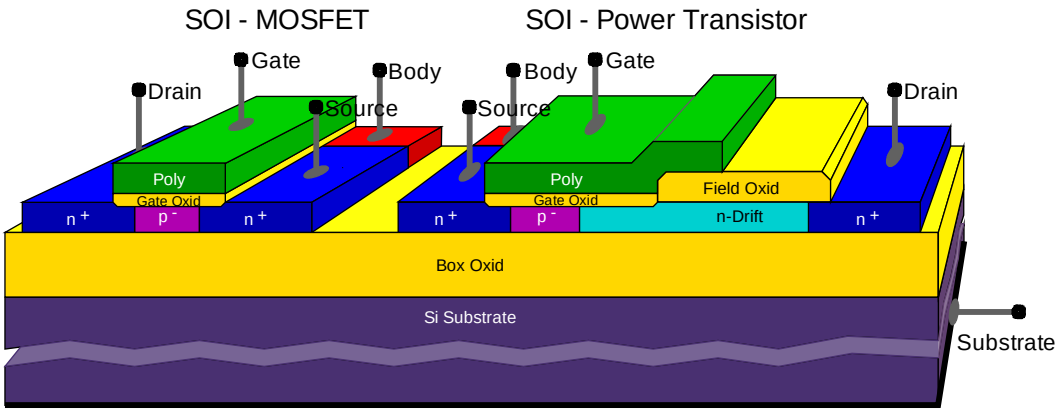

Fig.1: *Cross section of a SOI wafer*

A SOI wafer consists of three layers (Fig. 1). On the top a thin mono-crystalline silicon layer can be found above an oxide layer. This oxide layer is situated on a silicon wafer. The first very thin oxide layer is used as active layer, in which the

devices are realised. The further processing of the wafers does not differ from bulk CMOS except for one point: all devices are separated from each other by etching through the active layer down to the buried oxide, thereby reducing unwanted electrical interaction between them. Also in comparison to CMOS devices the buried oxide limits the vertical structure and the area of the pn-junctions is strongly reduced. The active area below the poly-silicon gate (body) is not necessarily connected in SOI devices. Leaving this area floating leads to a threshold voltage shift towards lower voltages during operation as the body area is charged up (kink effect). As it is in most cases desirable to suppress the kink effect, the body area is usually connected to ground for n-channel devices and to supply voltage for p-channel transistors. These devices are called "body tied", the others known as "floating body".

3. EEPROM CELL DEVELOPMENT

An EEPROM memory cell consists of a floating gate transistor (storage transistor) and a select transistor to allow access to specific cells in a memory cell array. Information is stored in form of a threshold voltage change, which is induced by charge moving onto or being removed from the floating gate via Fowler-Nordheim tunnelling through the thin oxide (11 nm) at the injector window. The select transistor has to be a high-voltage device because it has to withstand the programming voltage of 12V-18V. To avoid parasitic action due to the floating body effect, both storage and select transistor have to include body ties in form of film contacts.

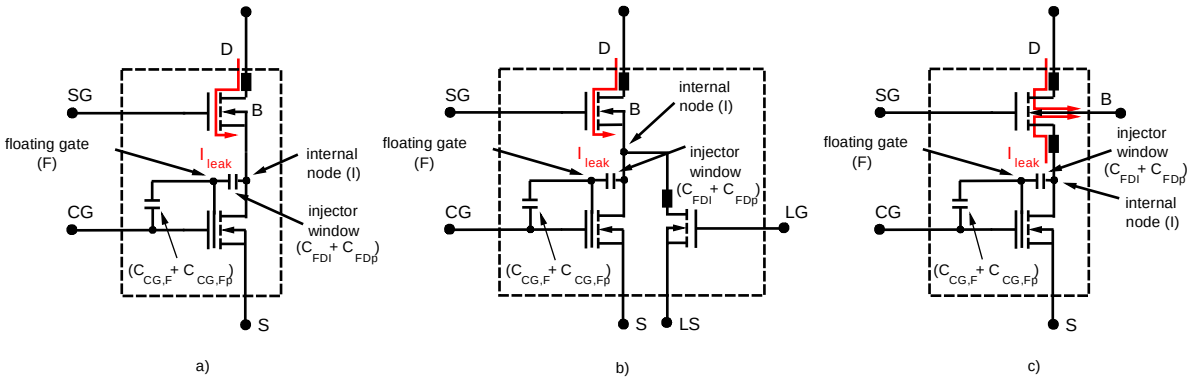

Fig.2: *(a) Standard [1], (b) standard improved [3] and (c) novel EEPROM cell*

Two types of cells, differing in the way the body node of the select transistor is connected, were examined. Cell 1 is the traditional EEPROM cell design transferred to SOI technology [1]. The select transistor of this memory cell is a body-tied-to-

source device (Fig. 2). Although this method is very useful at low temperatures it causes new problems at temperatures higher than 150˚C, where the increased leakage current from drain to body can lead to data loss when neighbouring cells at the same bit line are written (Fig. 3). This current charges the source area as it is connected to body, leading to an open select transistor regardless of the gate voltage applied. The reach through from drain to source can be compensated by an extra transistor connecting the internal node of the EEPROM cell to ground when the cell is deselected [3]. The effect is efficiently suppressed by the extra device, resulting in a three-transistor memory cell and therefore increased cell area consumption.

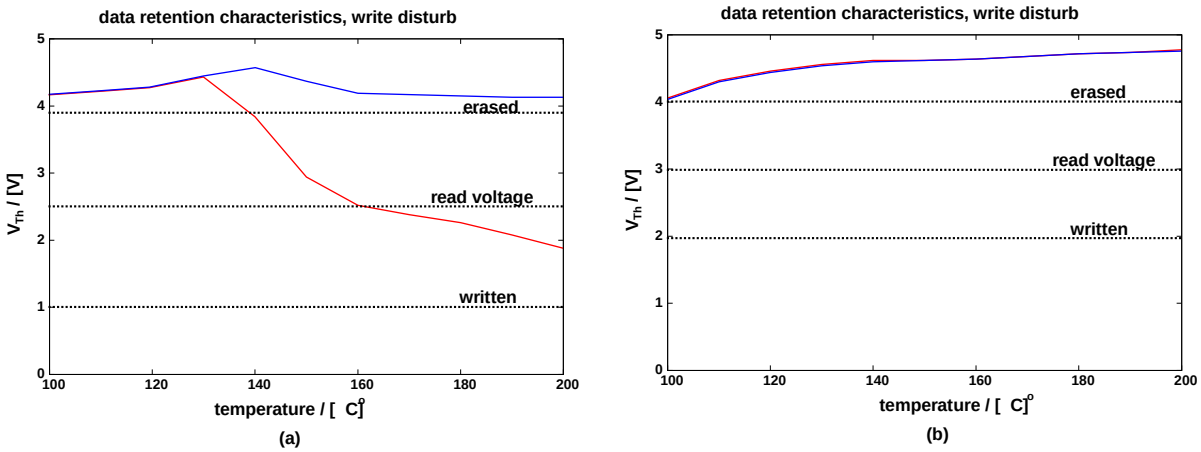

Fig.3: *Data retention characteristics during write disturb test: (a) standard and (b) novel EEPROM cell*

To avoid an increase in area consumption, a low leakage high-voltage transistor design was developed. This device features a separated body contact and extension areas at both source and drain. It allows reliable switching in all operating states. Furthermore, data loss at high temperatures can be suppressed as leakage currents from drain can discharge through the body. During read, erase and idle mode, the body node is connected to ground. This will tie the floating drain of the storage transistor to a maximum of one diode forward bias voltage, preventing charge loss from the floating gate and thereby data loss reliably. A memory cell featuring this select transistor is well suited for application at high temperatures, even though the programming window of this cell is smaller compared to cell 1 and special care has to be taken when controlling the body to avoid breakdown (Tab. 1) [2].

	Write	Erase	Read
SG	V_{PP} + 1.5V	5V	5V
CG	0V	V_{PP}	V_R
D	V_{PP}	0V	0.1V
B	V_B	0V	0V
S	floating	0V	0V

Tab.1: *Operating conditions of an EEPROM cell with n-channel select transistor*

A minimal cell array (Fig. 4), consisting of two memory cells, was used to examine the unimpaired operation as well as the reliability of the cells in an EEPROM cell array. The memory cells are connected in exactly the same way as in the cell array of a memory chip. Within the array, the control gates and the body nodes of one word are connected. Also the select gates are conjunct forming the word line. The drain nodes (bit lines) are kept separated, allowing access to each single memory bit. For each memory block, all source nodes are conjunct.

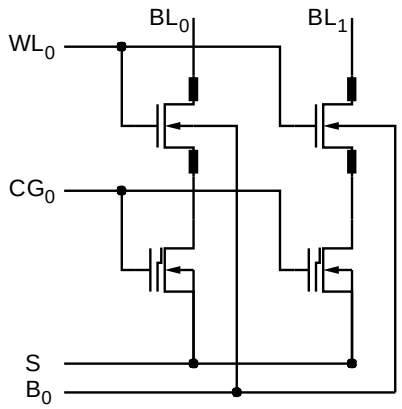

Fig. 4: *Minimal cell array used for reliability testing*

The structures were subjected to reliability tests to compare their data-retention and data-endurance values. For the data-retention tests 10 dies of one wafer were selected and one double cell (minimal matrix) of each kind of cell was programmed with the binary value “10”. Subsequently the wafer was baked for 22h at 250°C, after every few hours the threshold voltage of the cells was measured. The programming window of all cells decreased, but only in few cases by more than 10%.

For the data-endurance test the EEPROM cells were subjected to cycles of erasing both cells and writing “11” to the minimal matrix. After each step the programming window was measured by determining the threshold voltage in written and erased state.

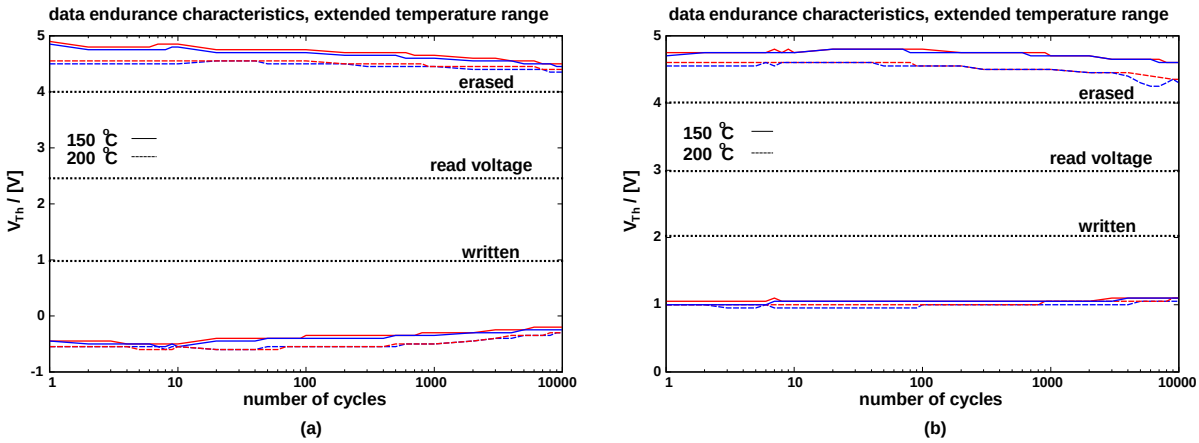

Fig. 5: *Data endurance characteristics: (a) standard and (b) novel EEPROM cell*

A cell is considered damaged, when the threshold voltage window is too narrow to distinguish these states. For both types of cells more than 10.000 cycles were possible at 200°C (Fig. 5). At room temperature more than 100.000 cycles can be reached.

4. CONCLUSIONS

Two EEPROM cell designs with different select transistors were developed. Measurements and comparison of cell properties have shown that a select transistor featuring a separate body contact improves the data retention behaviour of an EEPROM cell in an extended temperature range while the already good data endurance behaviour remains untouched.

References

[1] D. Gogl, G. Burbach, H.-L. Fiedler, M. Verbeck, and C. Zimmermann, "A single-poly EEPROM cell in SIMOX technology for high-temperature applications up to 250°C," in IEEE Electron Device Letters, vol.18, pp541-543, Nov. 1997

[2] S. Richter, D. Kirsten, D. Nuernbergk, St. Richter, "Embedded EEPROM design in PD-SOI for application in an extended temperature range", in Solid-State Electronics 49 (2005), pp.1484-1487.

[3] D. Gogl, H.-L. Fiedler, "A 1-kBit EEPROM in SIMOX technology for high temperature applications up to 250˚C," in IEEE J Solid State Circuits, vol. 35, pp. 1387-1395, Oct. 2000

Authors:

Dagmar Kirsten
Sonja Richter
Dr. Dirk Nuernbergk

IMMS gGmbH, Ehrenbergstr. 27, 98693 Ilmenau
E-mail: dagmar.kirsten@imms.de

Steffen Richter

X-FAB Semiconductor Foundries AG,
Haarbergstr. 67, 99099 Erfurt